

FIG. 1A

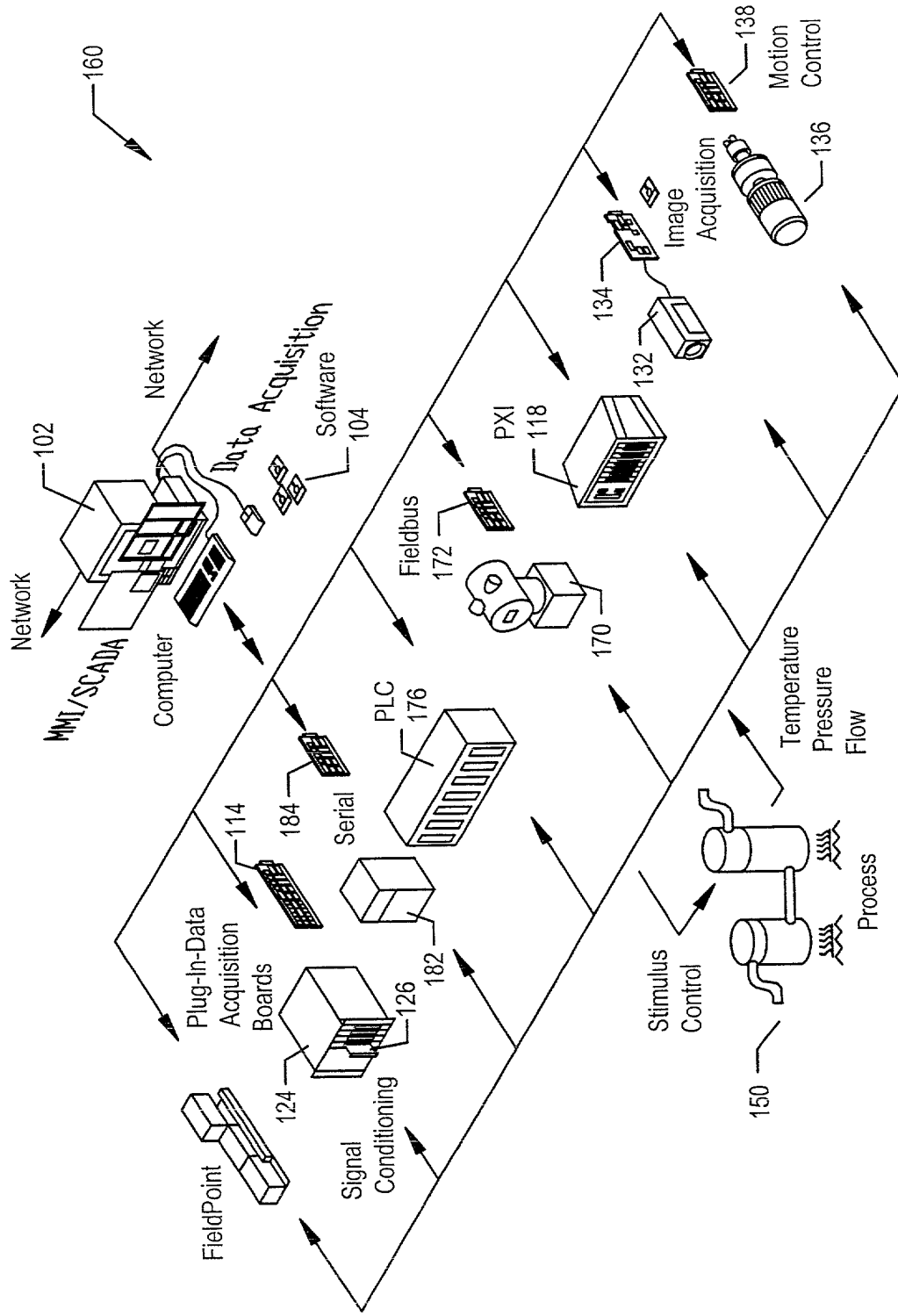


FIG. 1B

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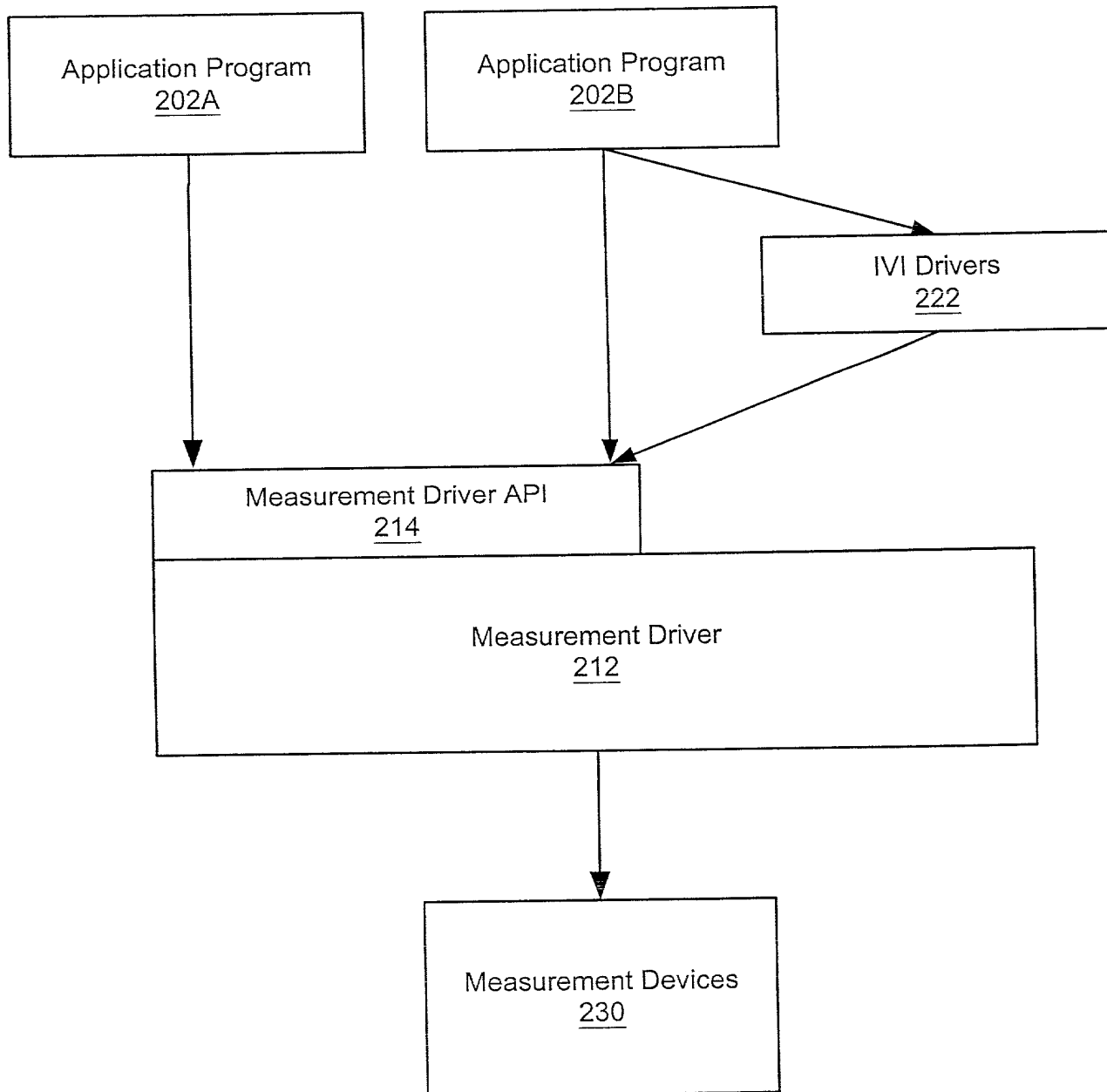


Figure 3

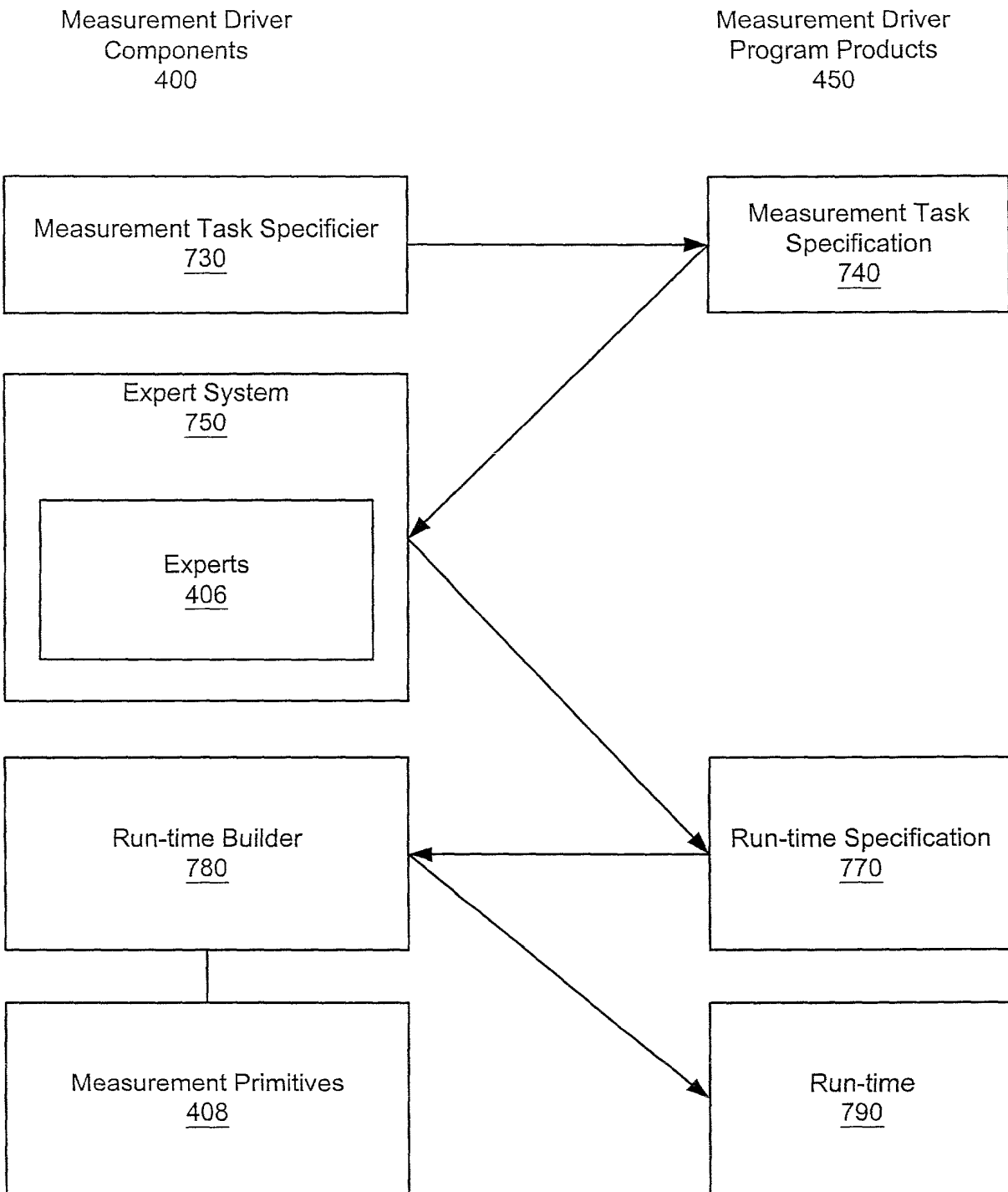


Figure 4

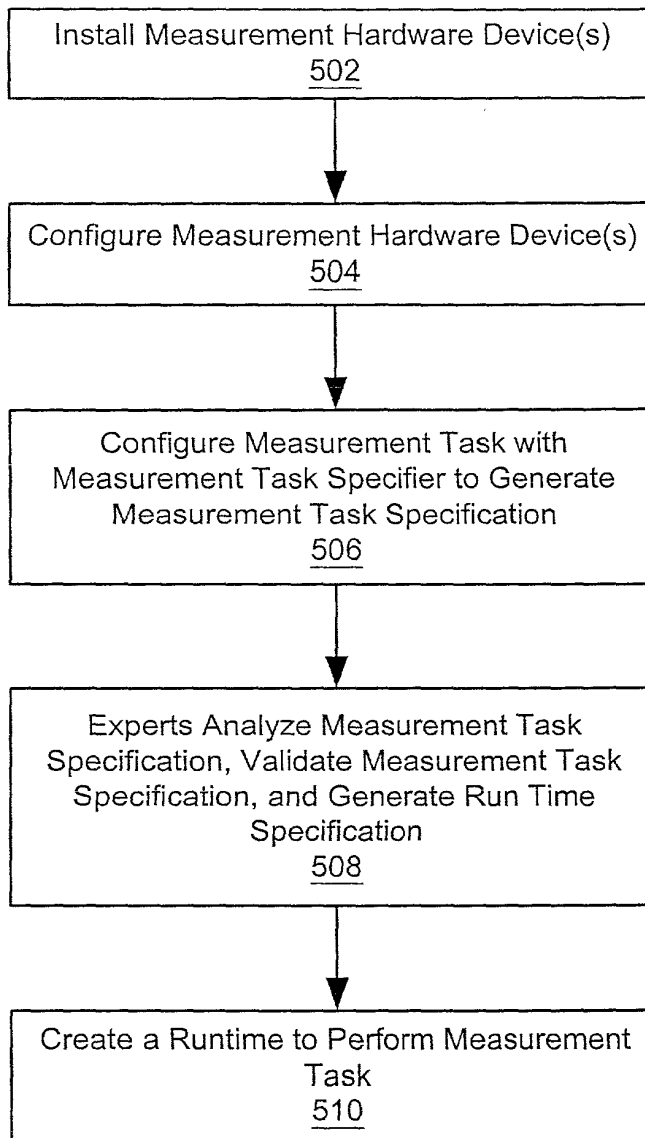
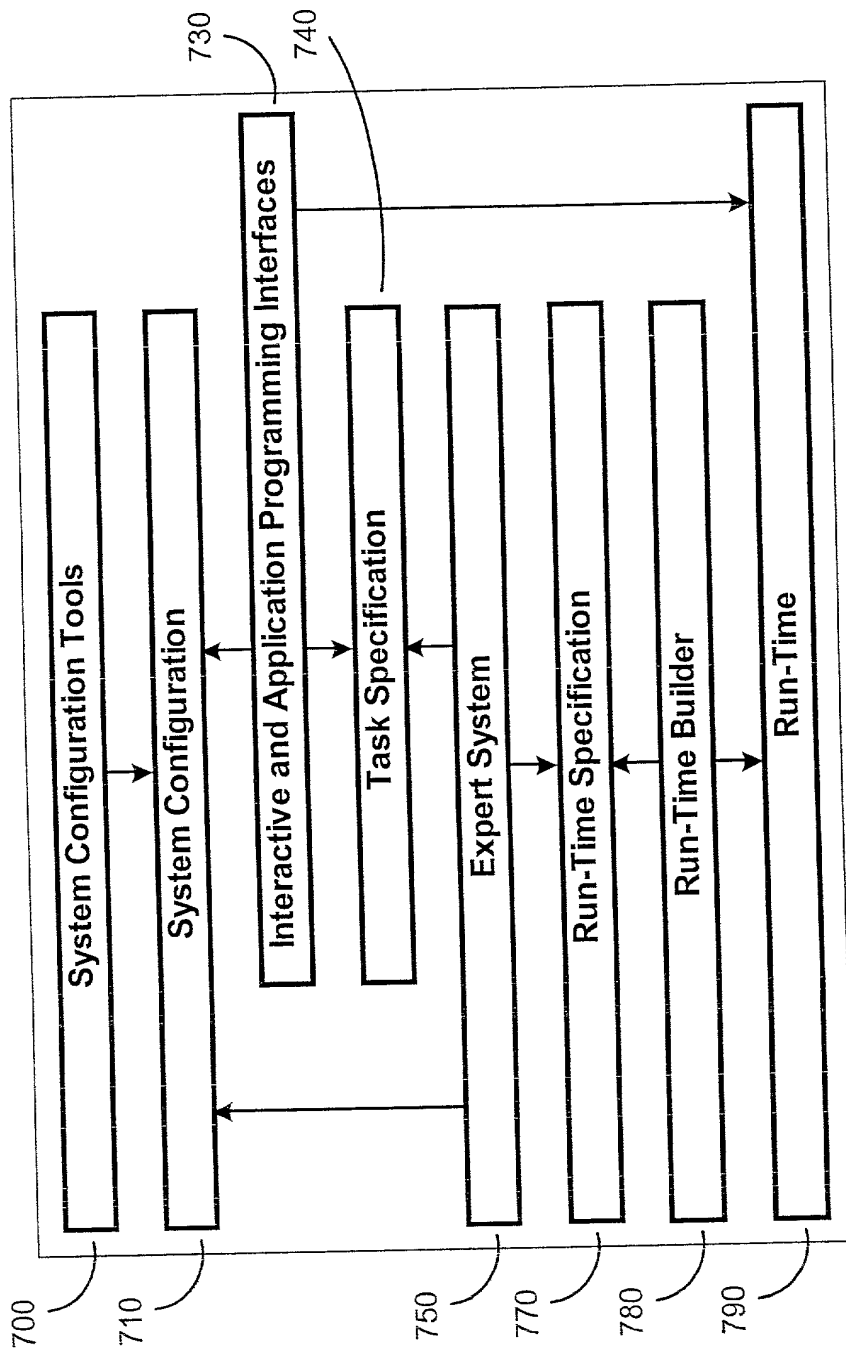


Figure 5



High-Level Architecture

Figure 6

# System Configuration and Task Specification

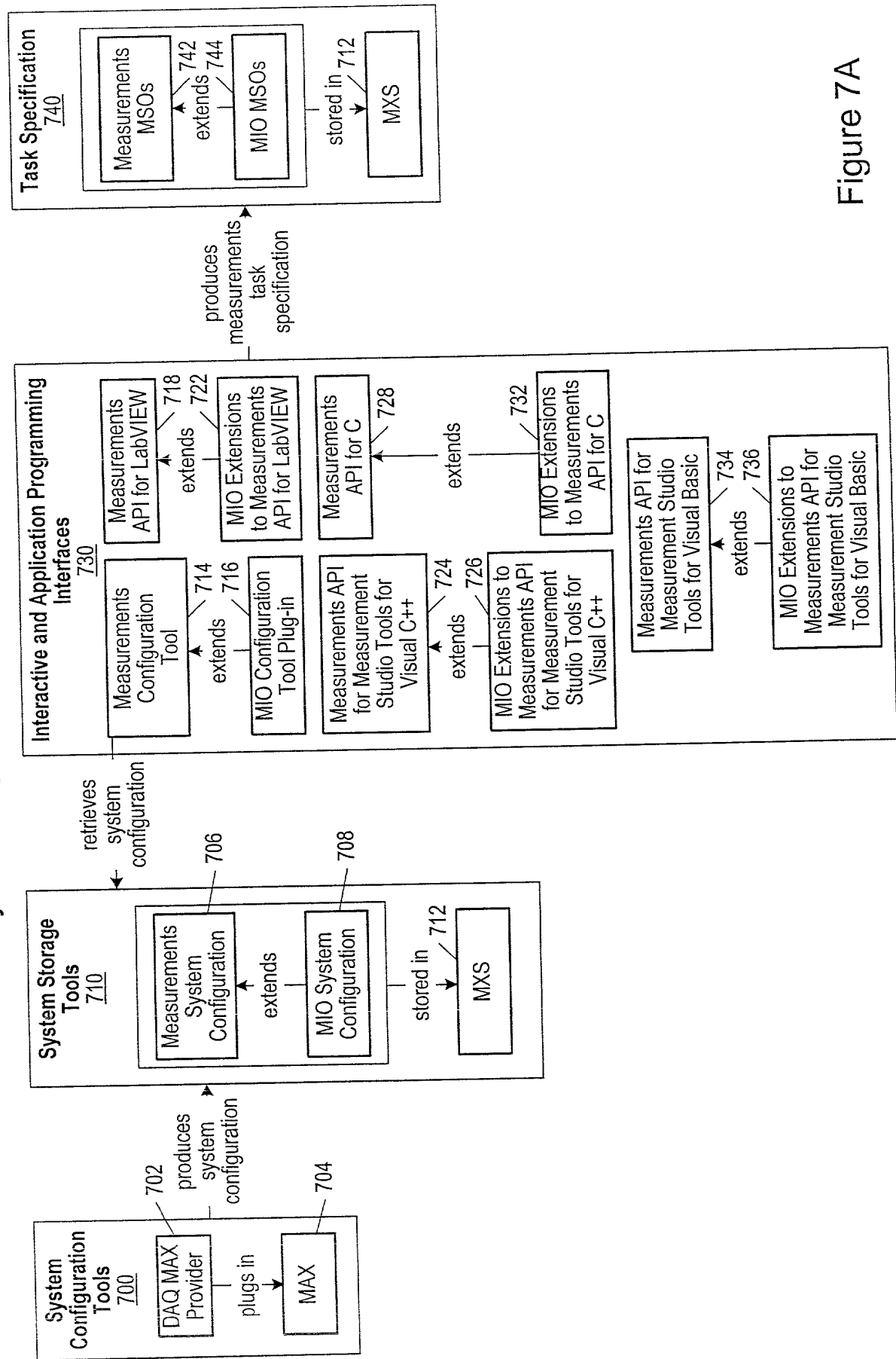


Figure 7A

# Compiling Task Specification to Task Run-time Specification

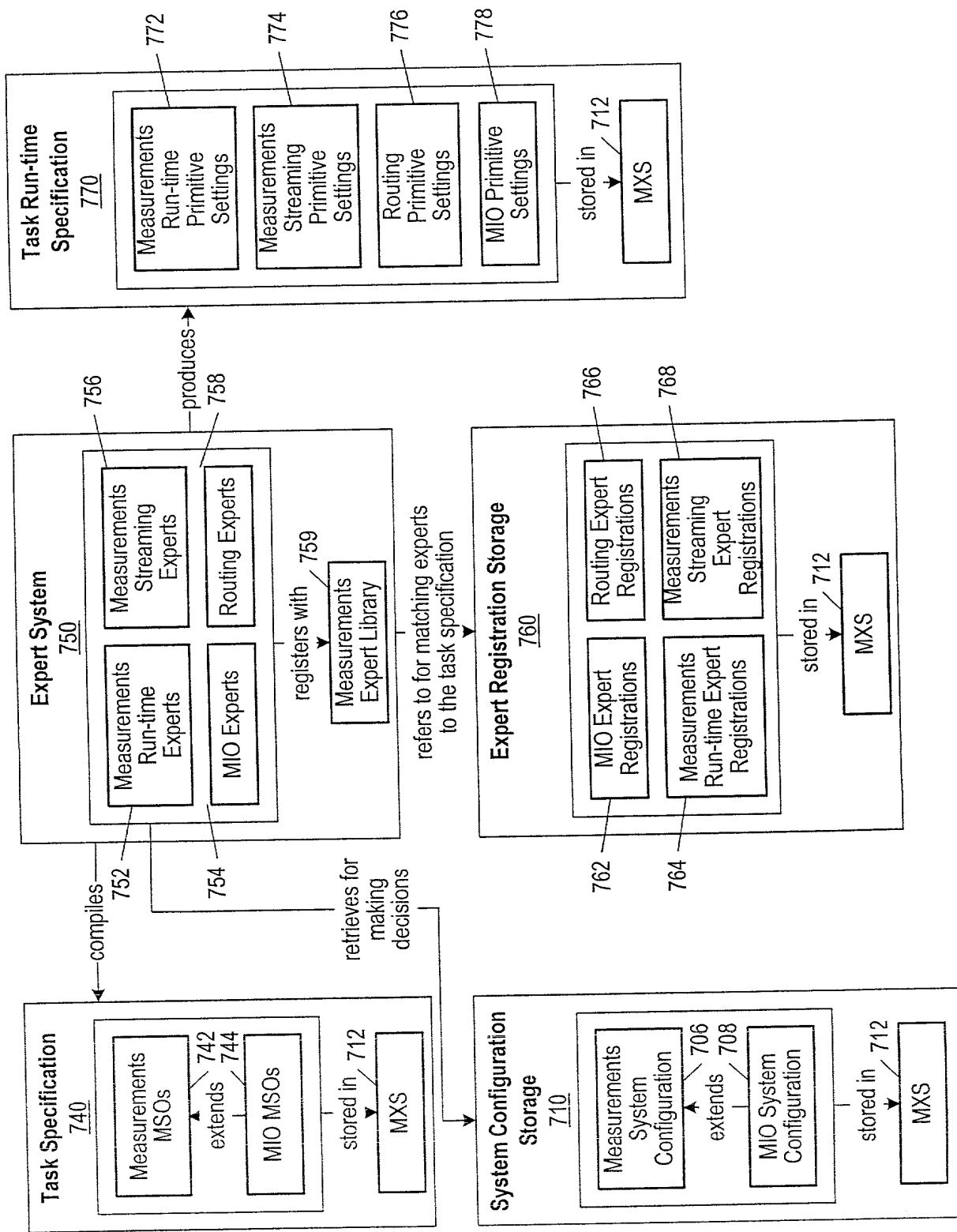


Figure 7B



# Building Task Run-time from Task Run-time Specification

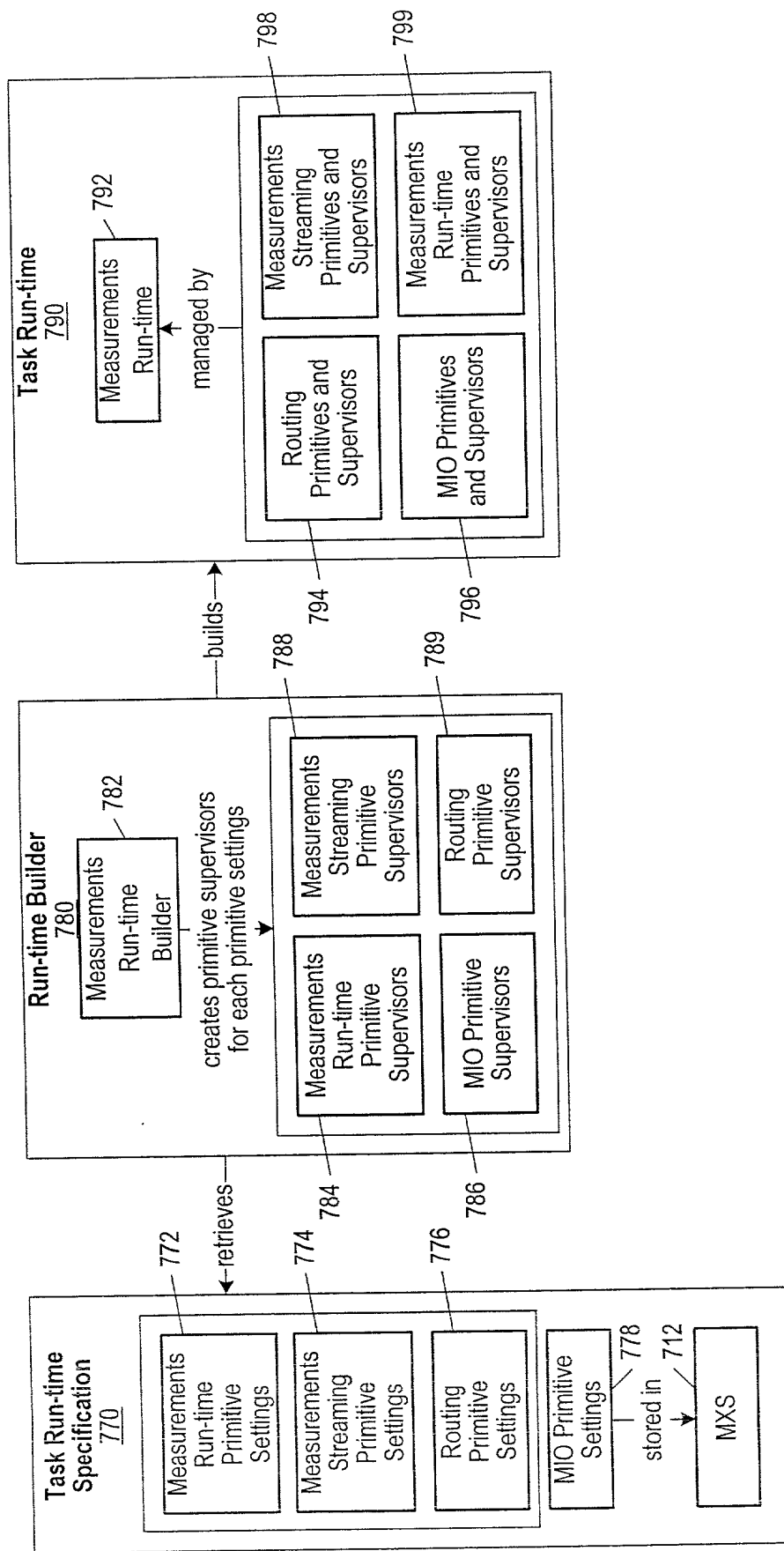


Figure 7C

## Executing Tasks

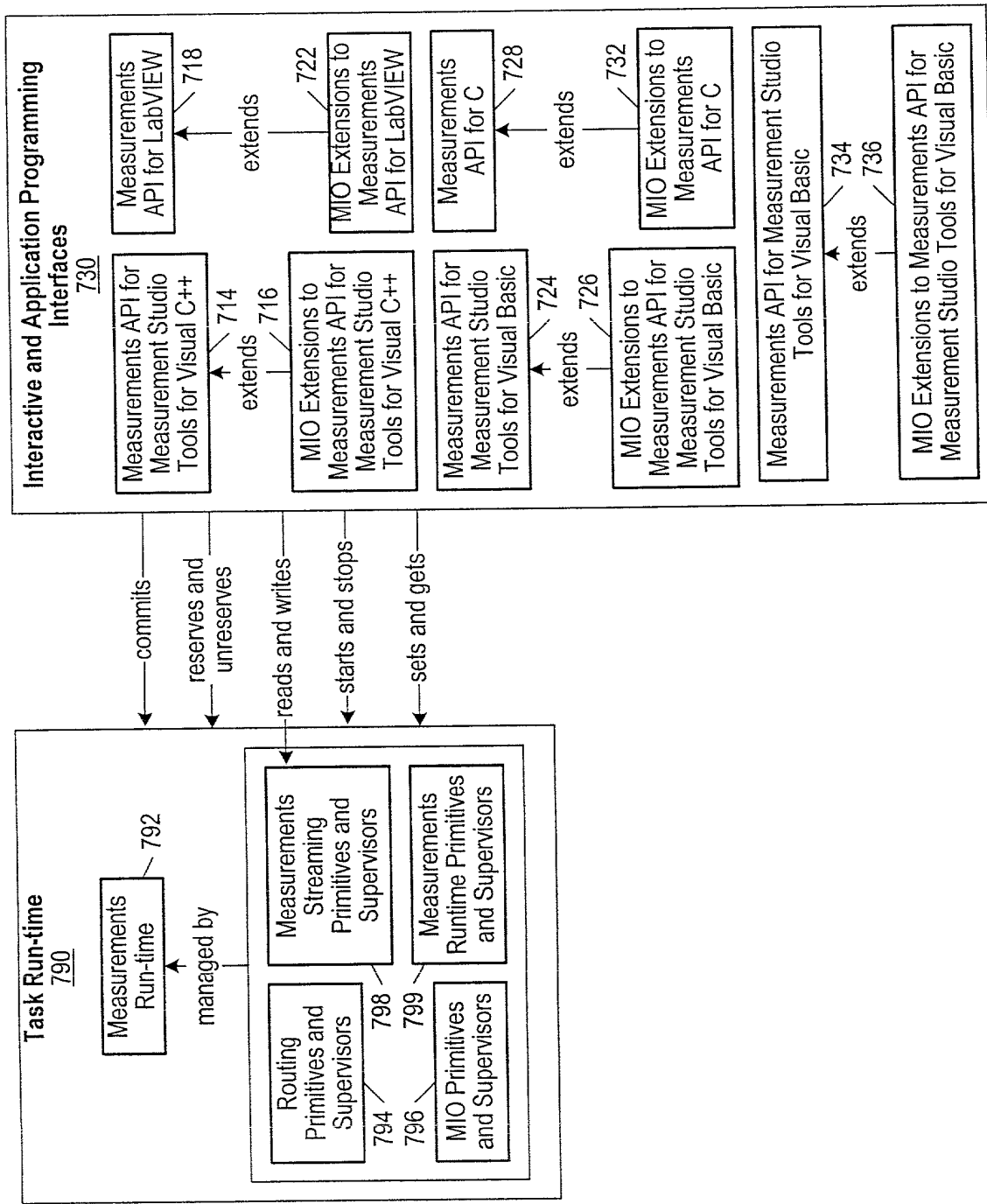


Figure 7D

# Packages for System Configuration and Task Specification

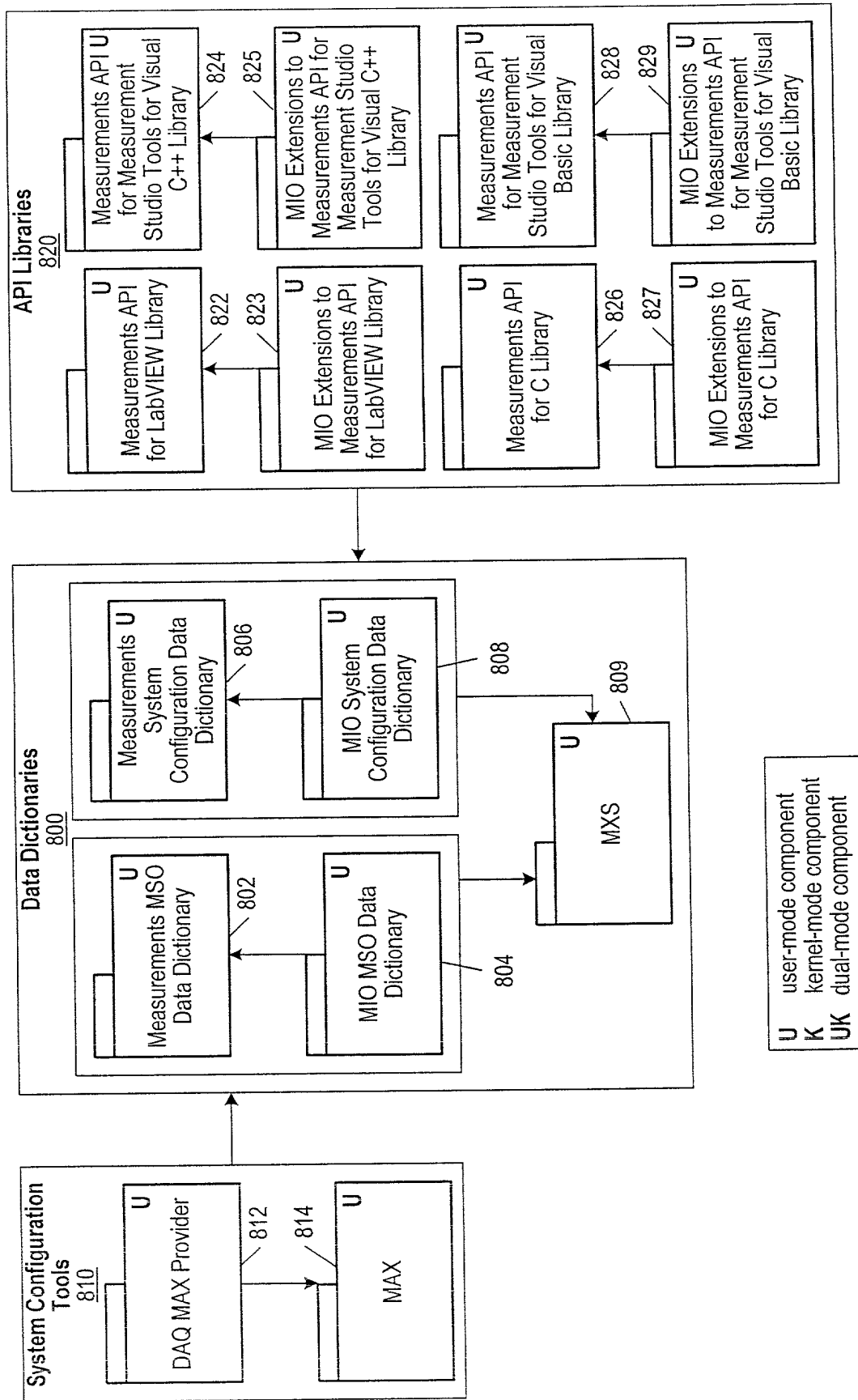


Figure 8A

# Packages for Compiling Task Specification to Run-time Specification

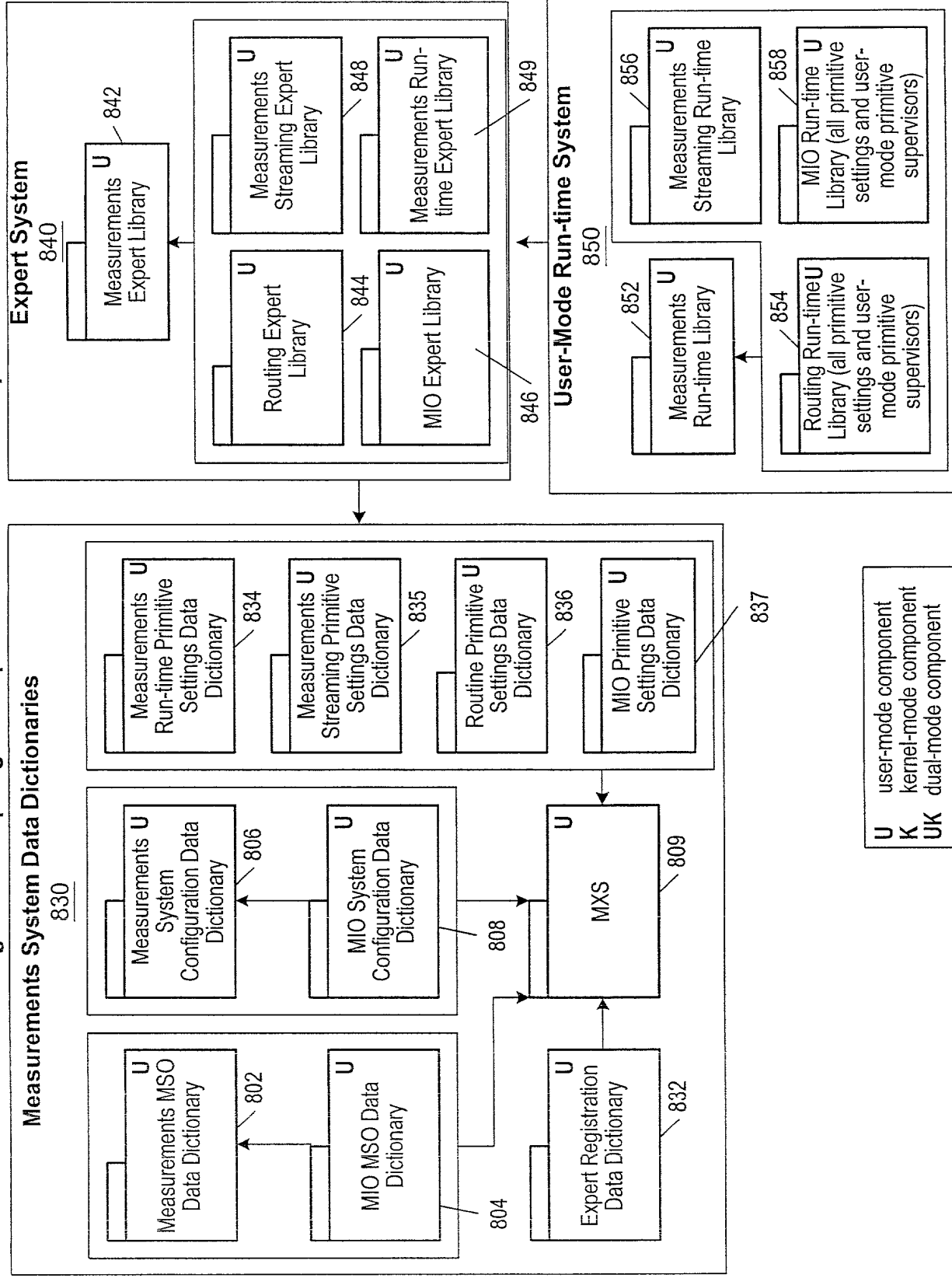


Figure 8B

Packages for Building Task Run-time from Run-time Specification

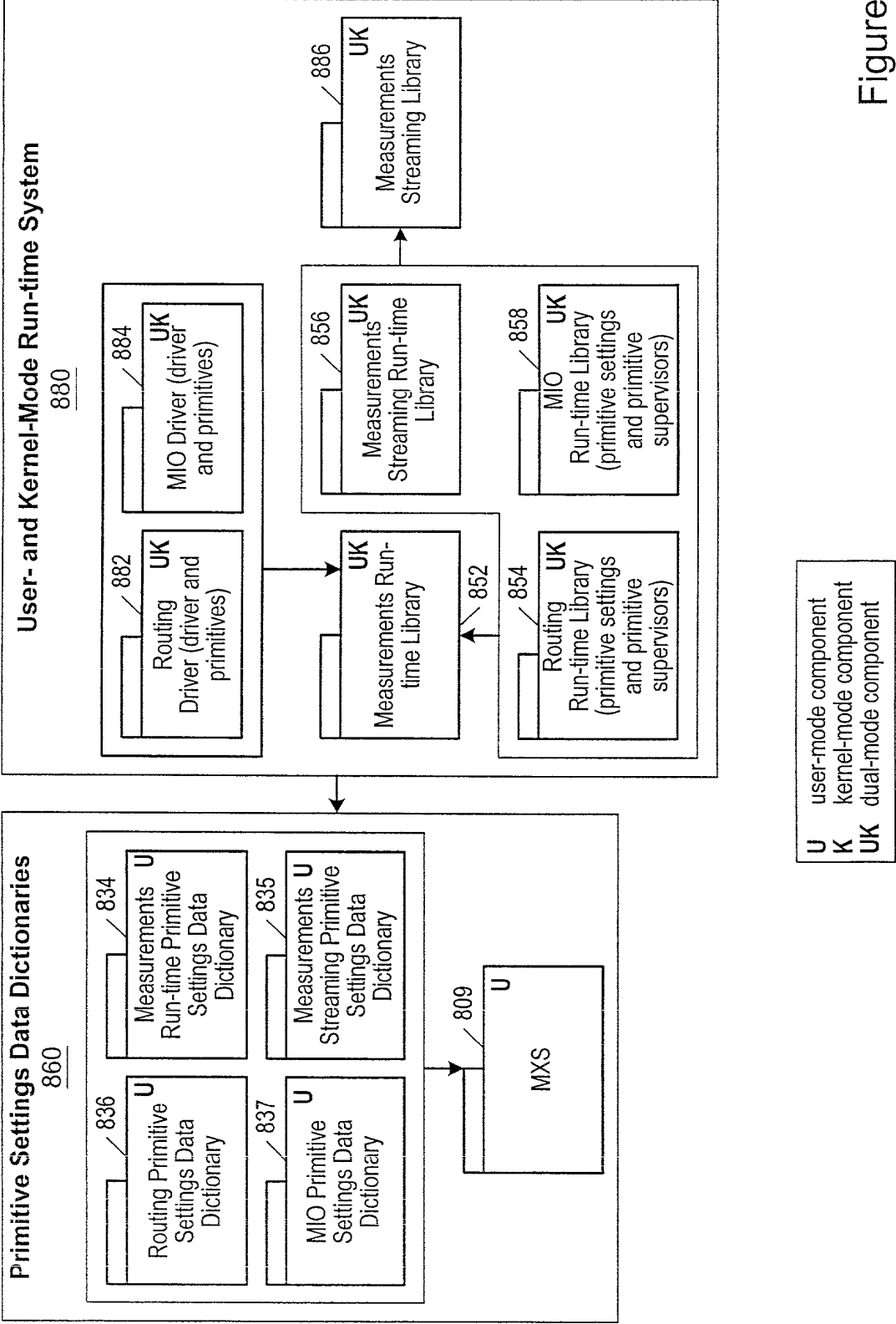


Figure 8C

# Packages for Executing Task Run-time

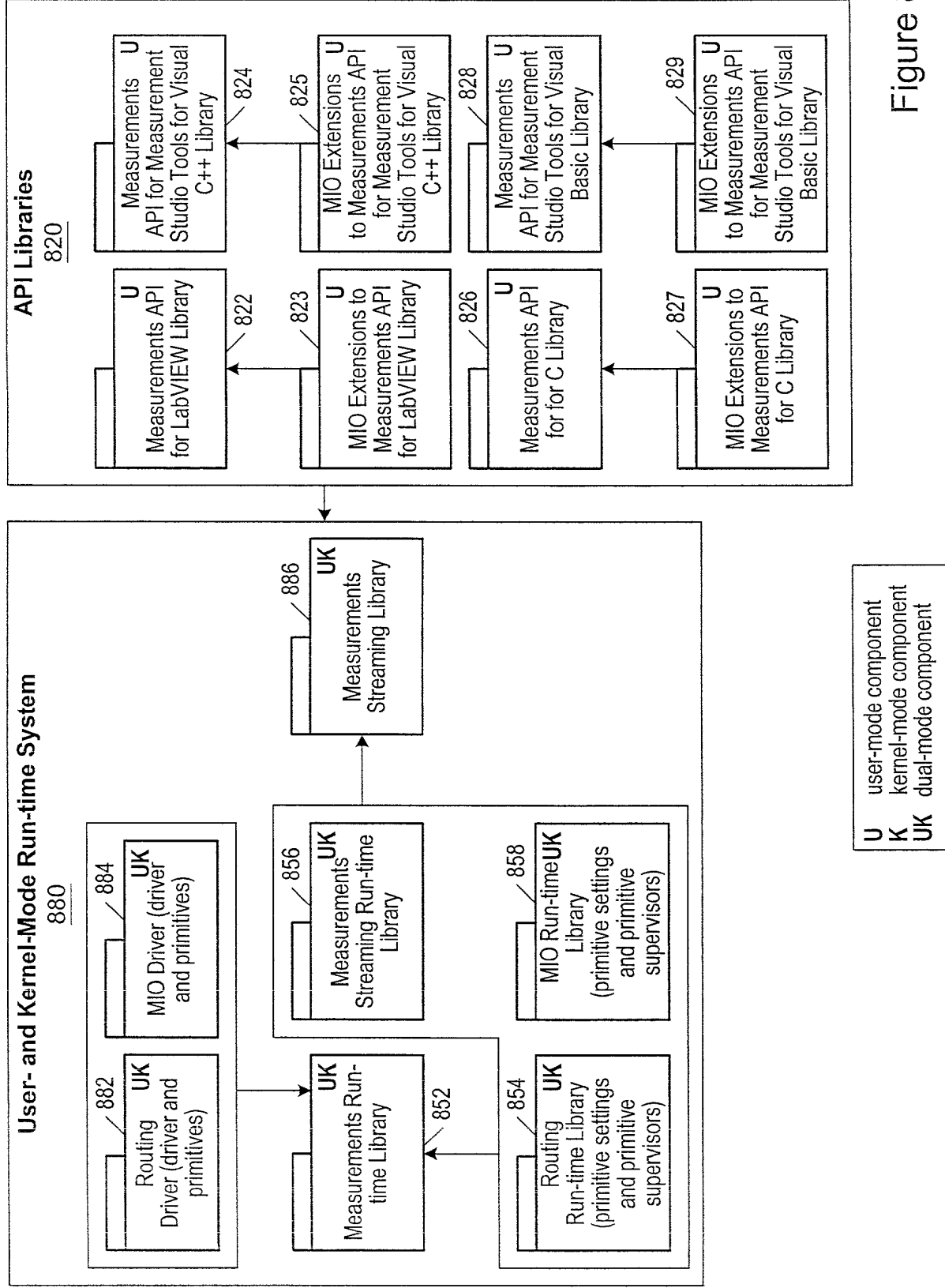


Figure 8D

# State Diagram for Measurement Tasks

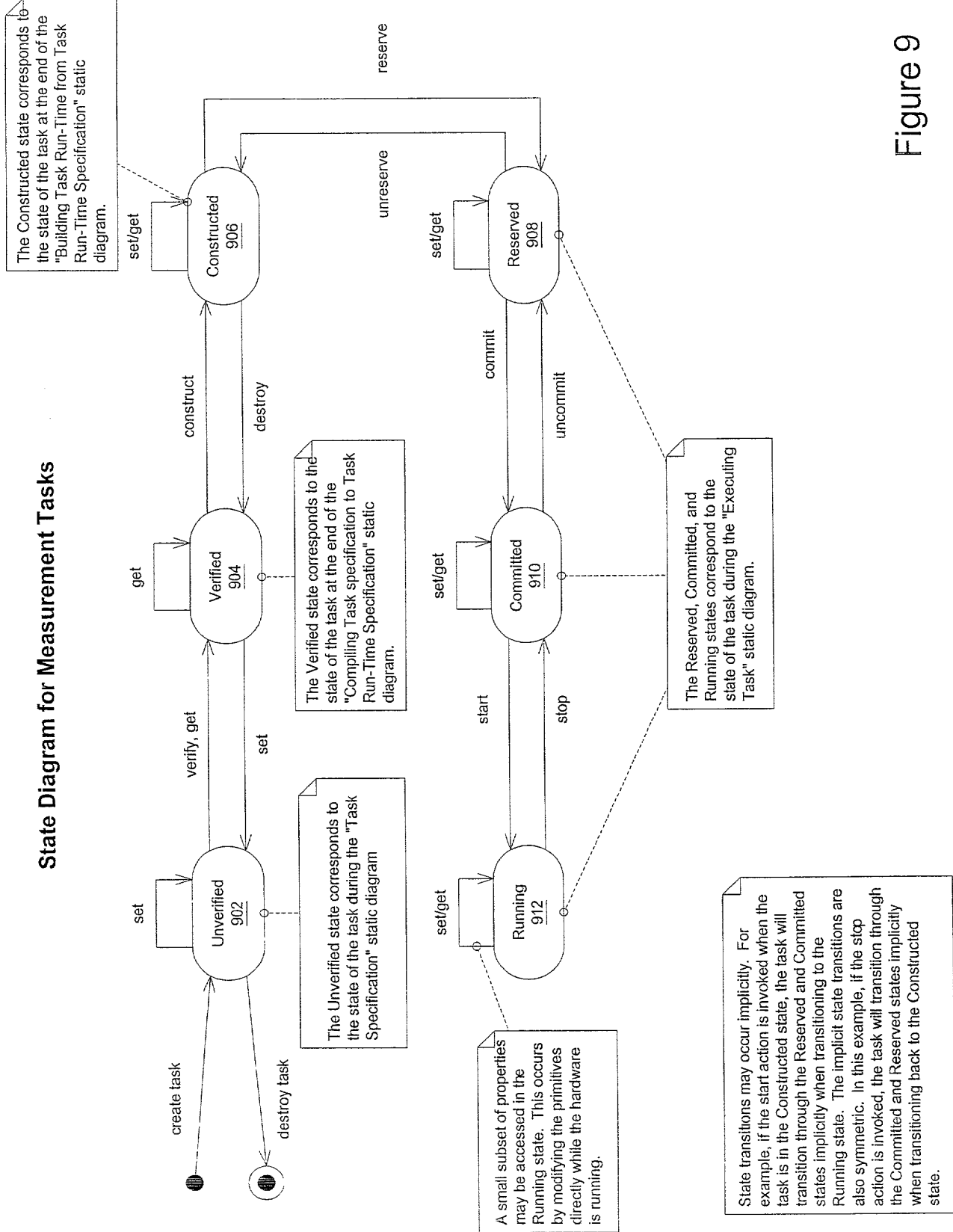


Figure 9

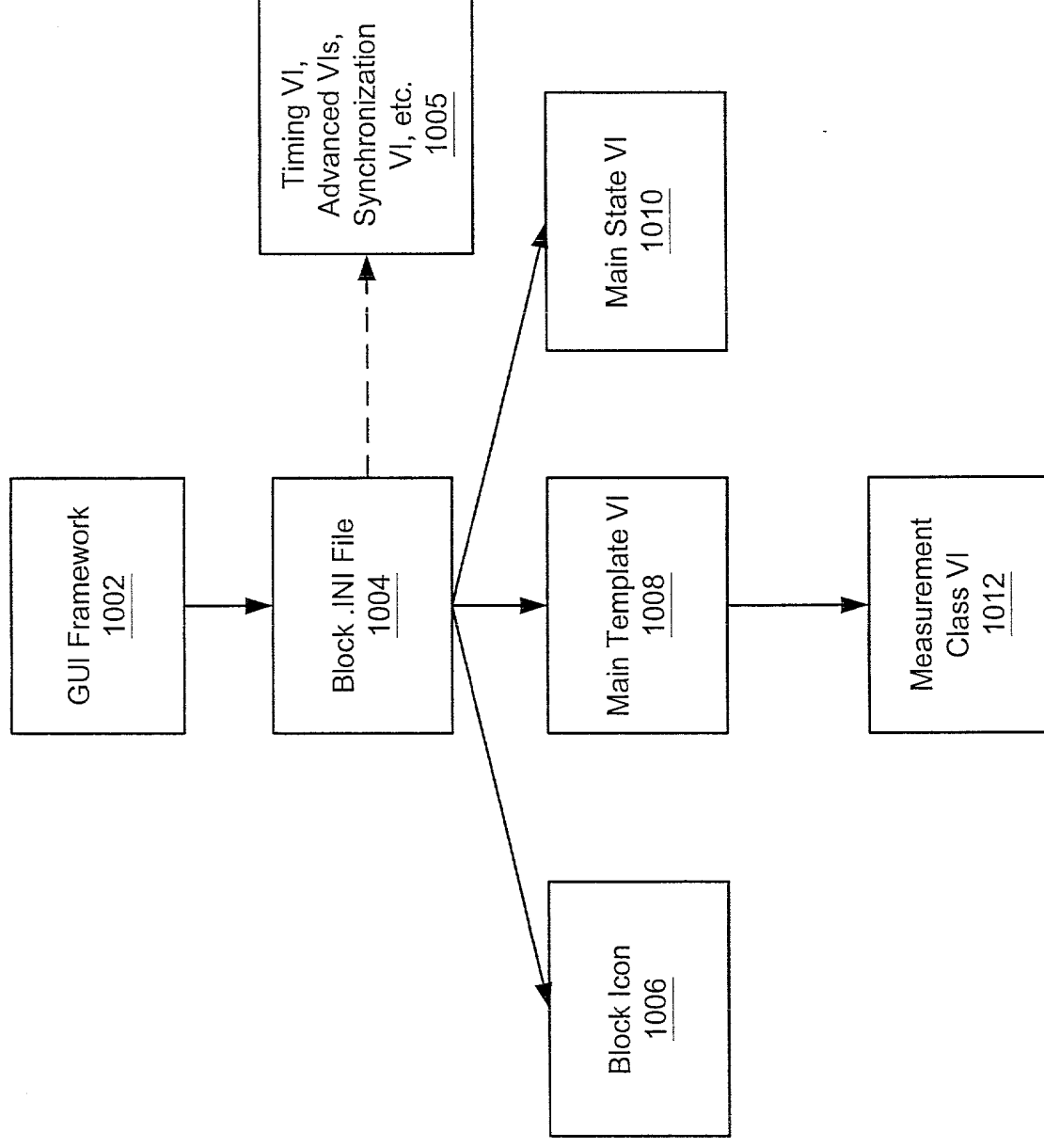


Figure 10



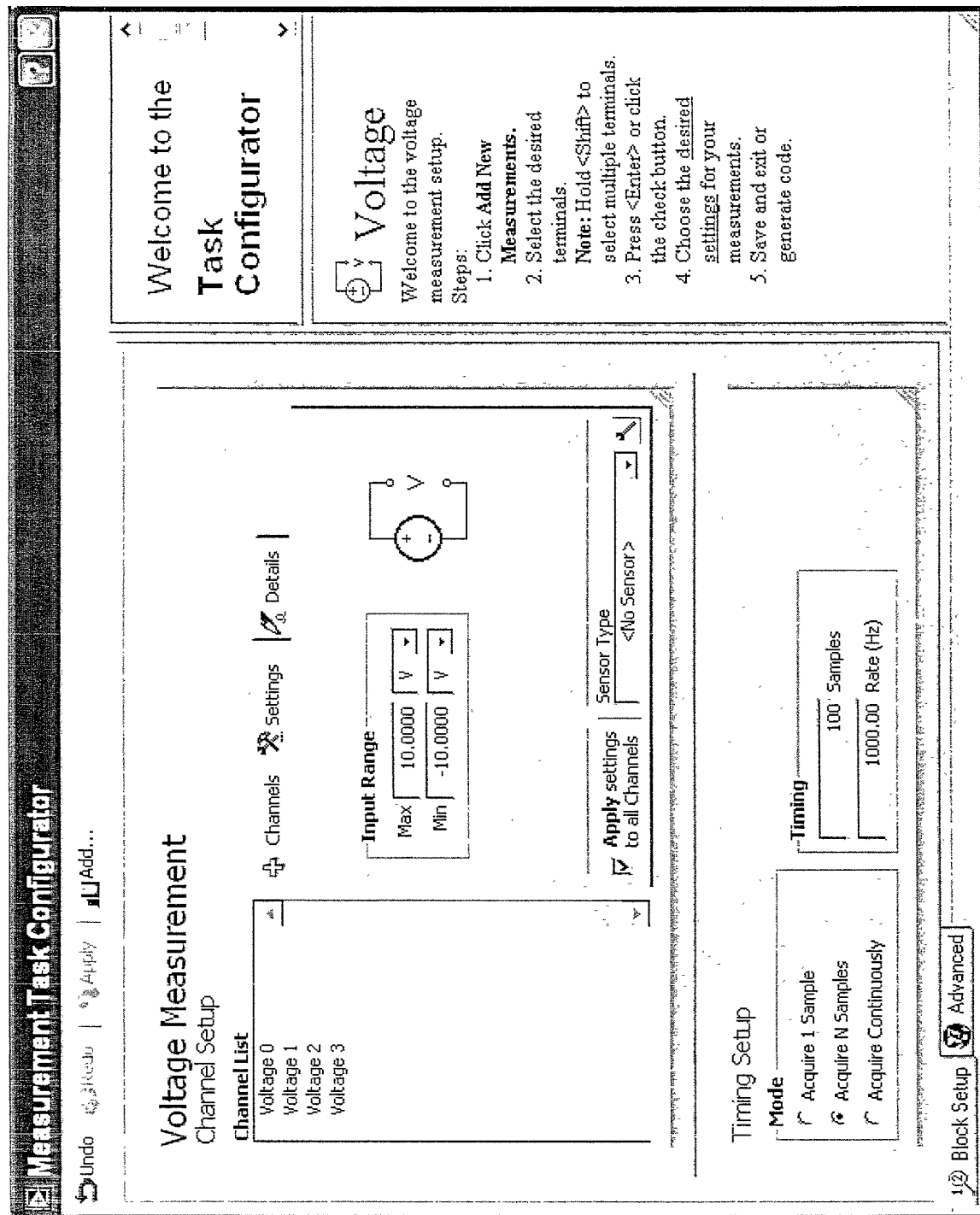


Figure 11

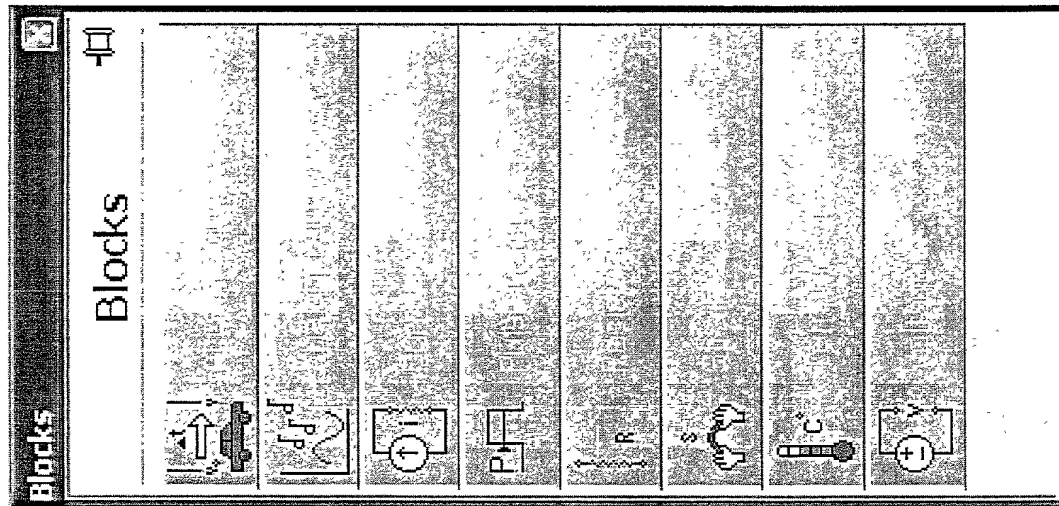


Figure 12A

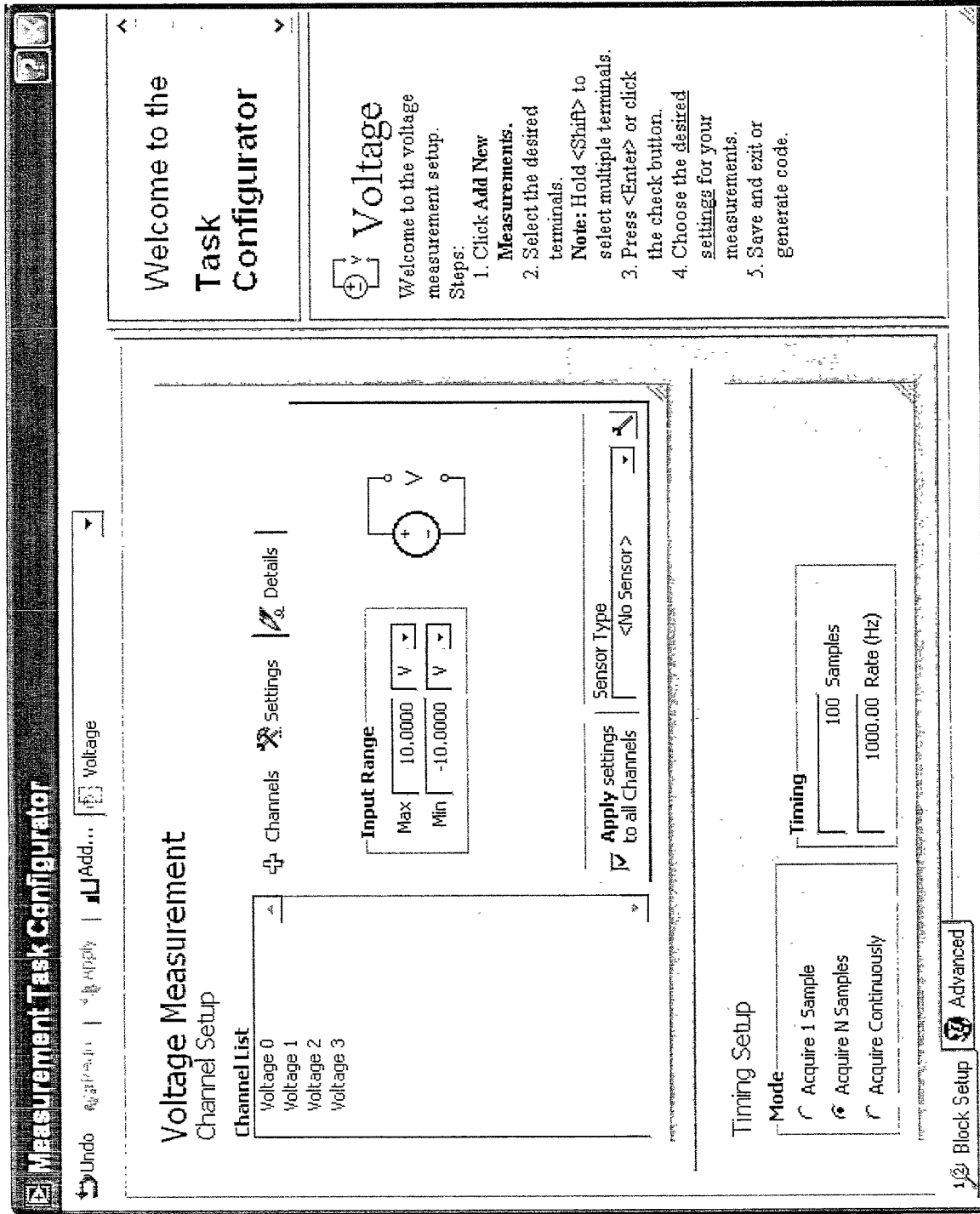


Figure 12B

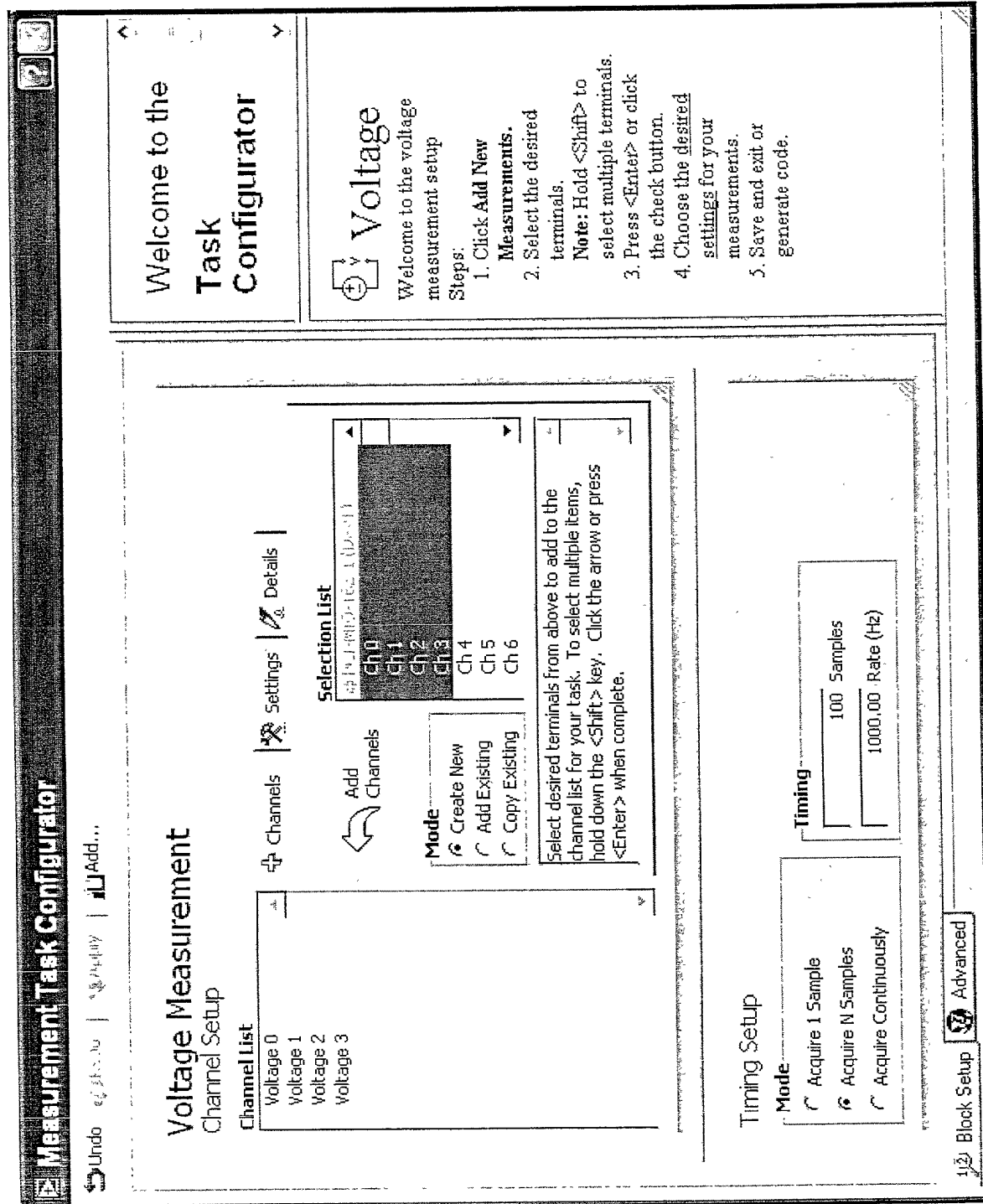


Figure 12C

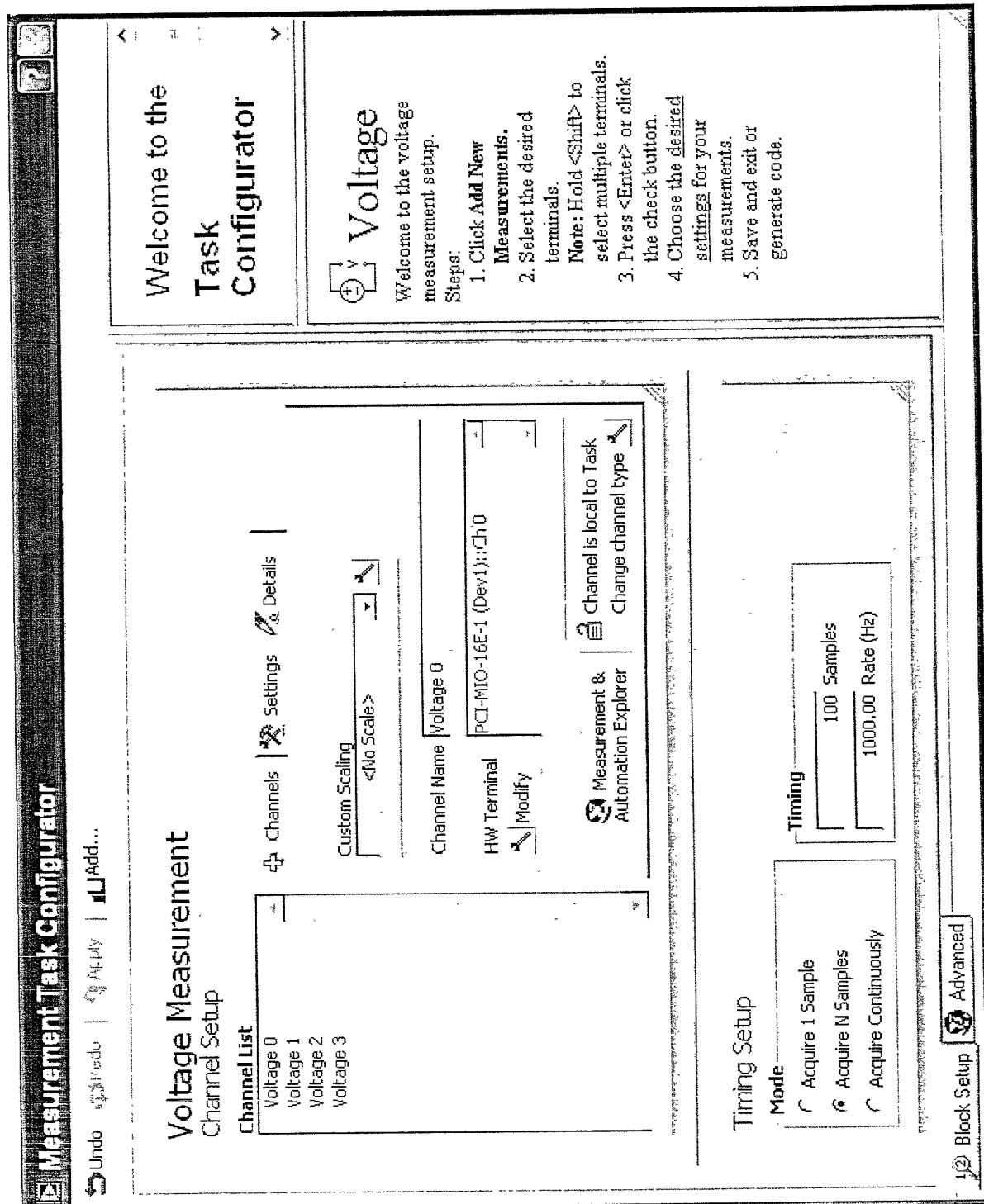


Figure 12D

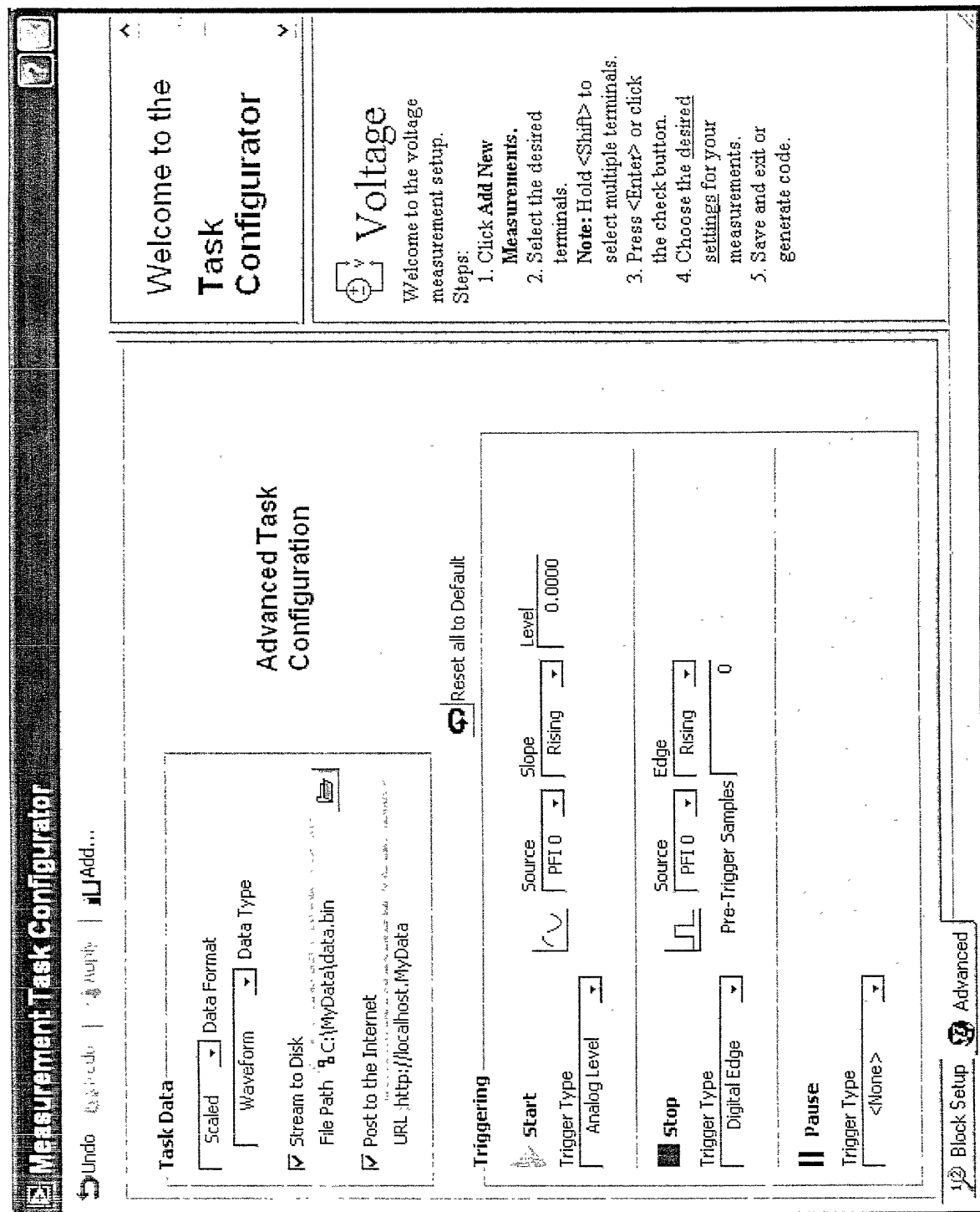


Figure 13

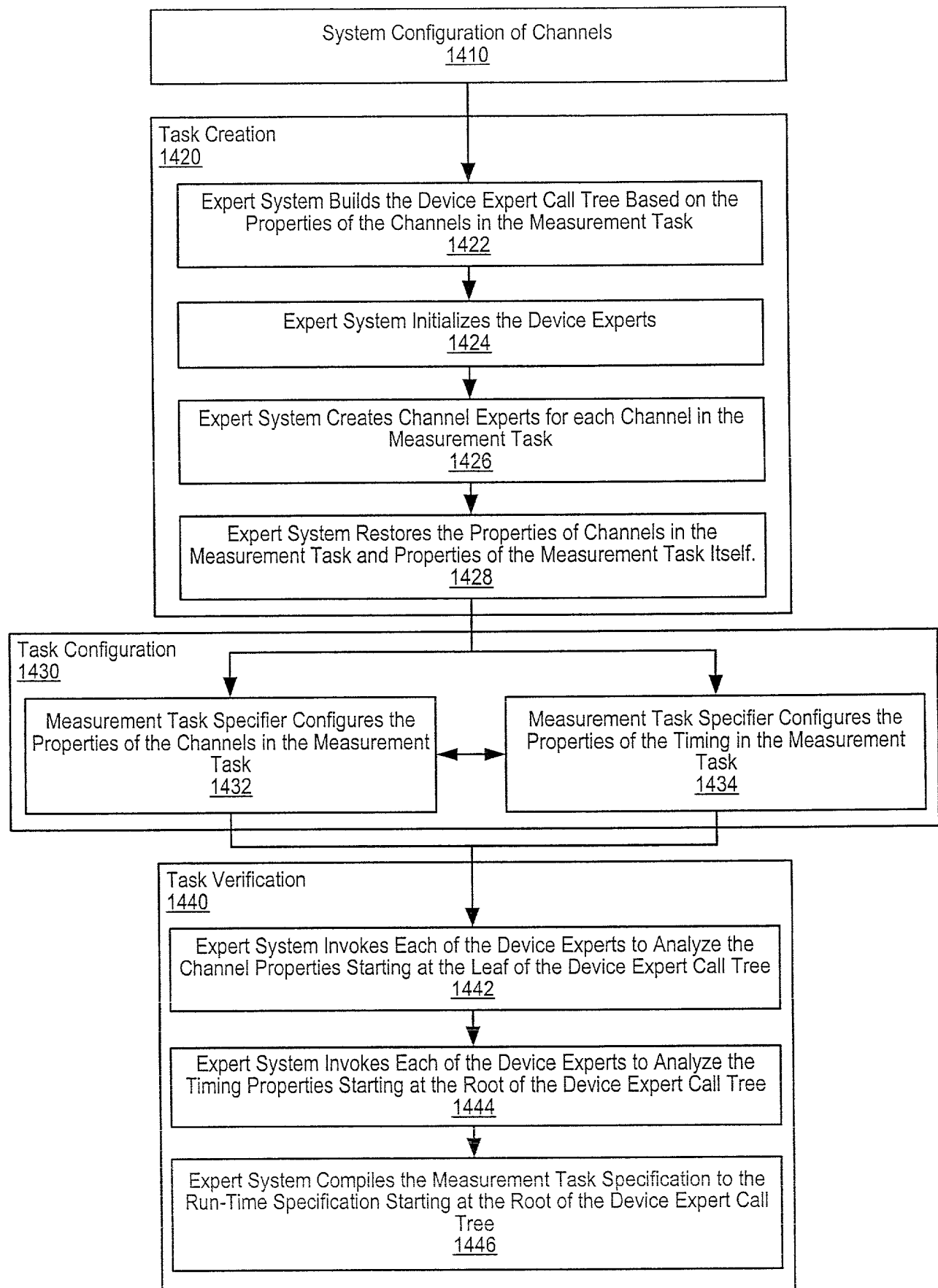


Figure 14

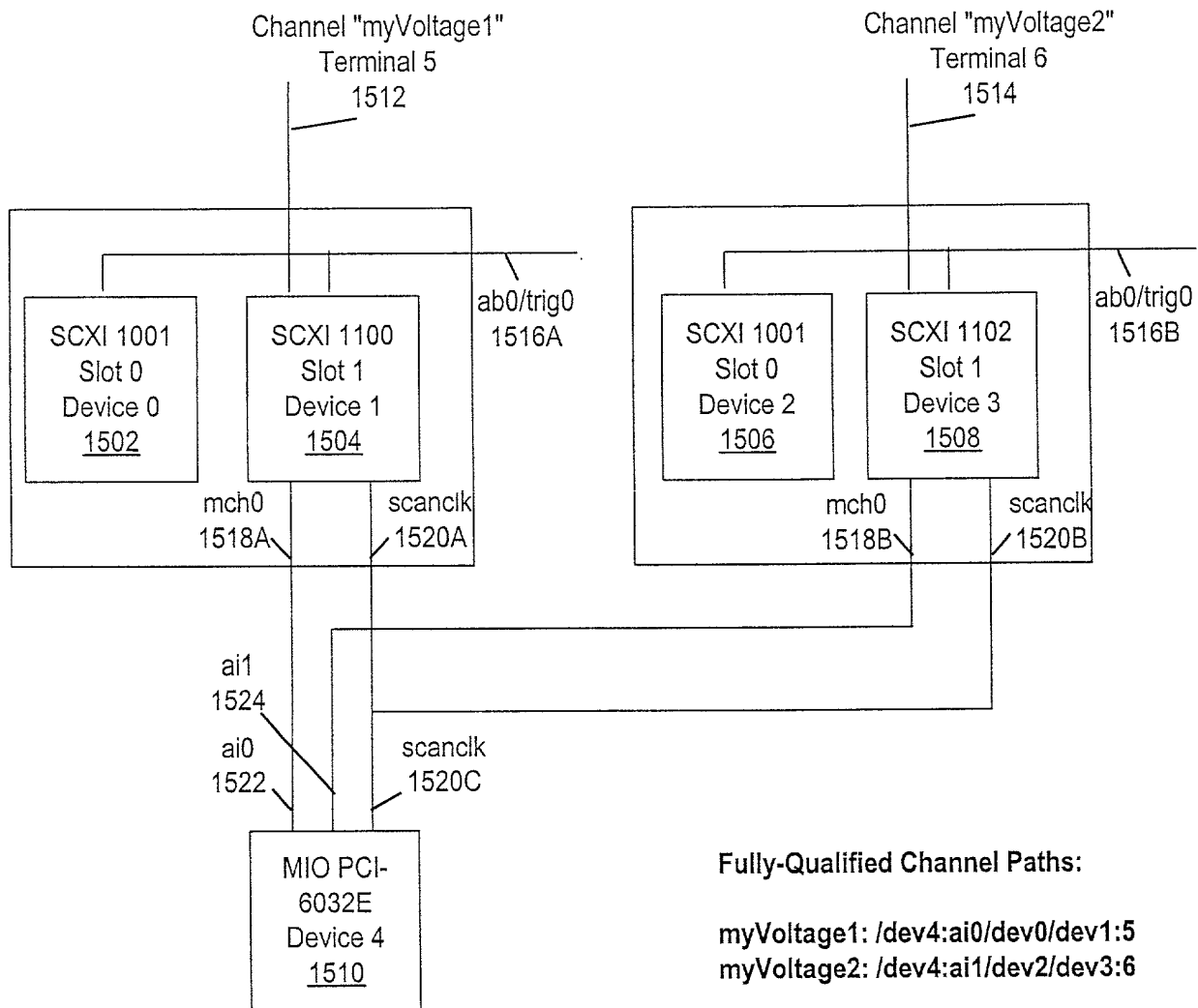


Figure 15



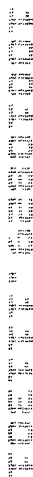
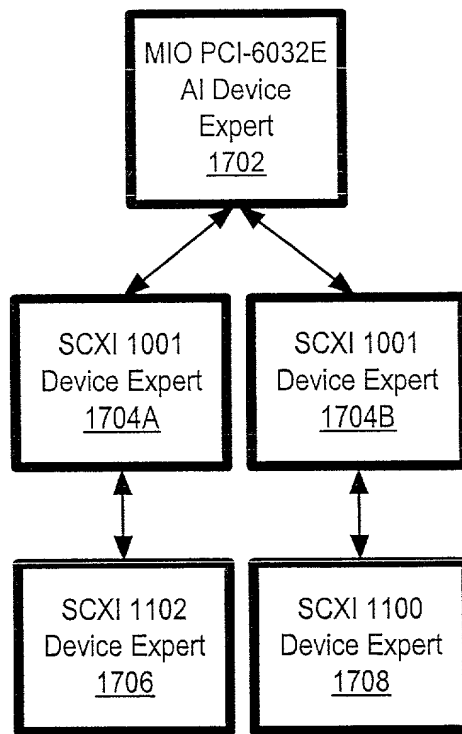


Figure 16



Create Device Expert Call Tree

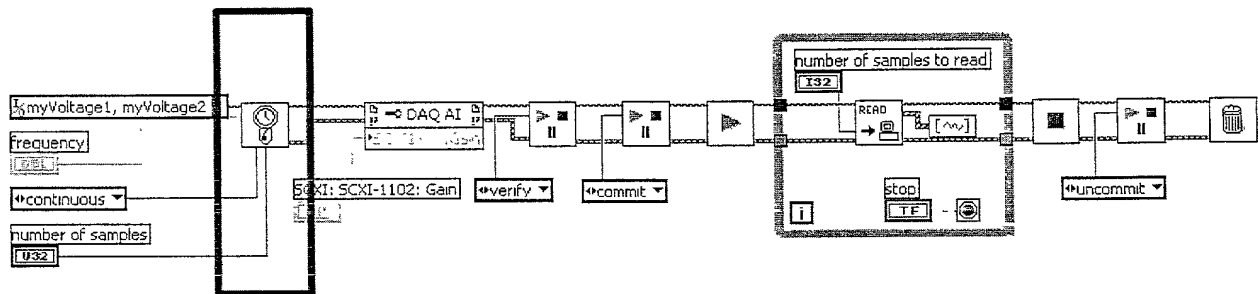
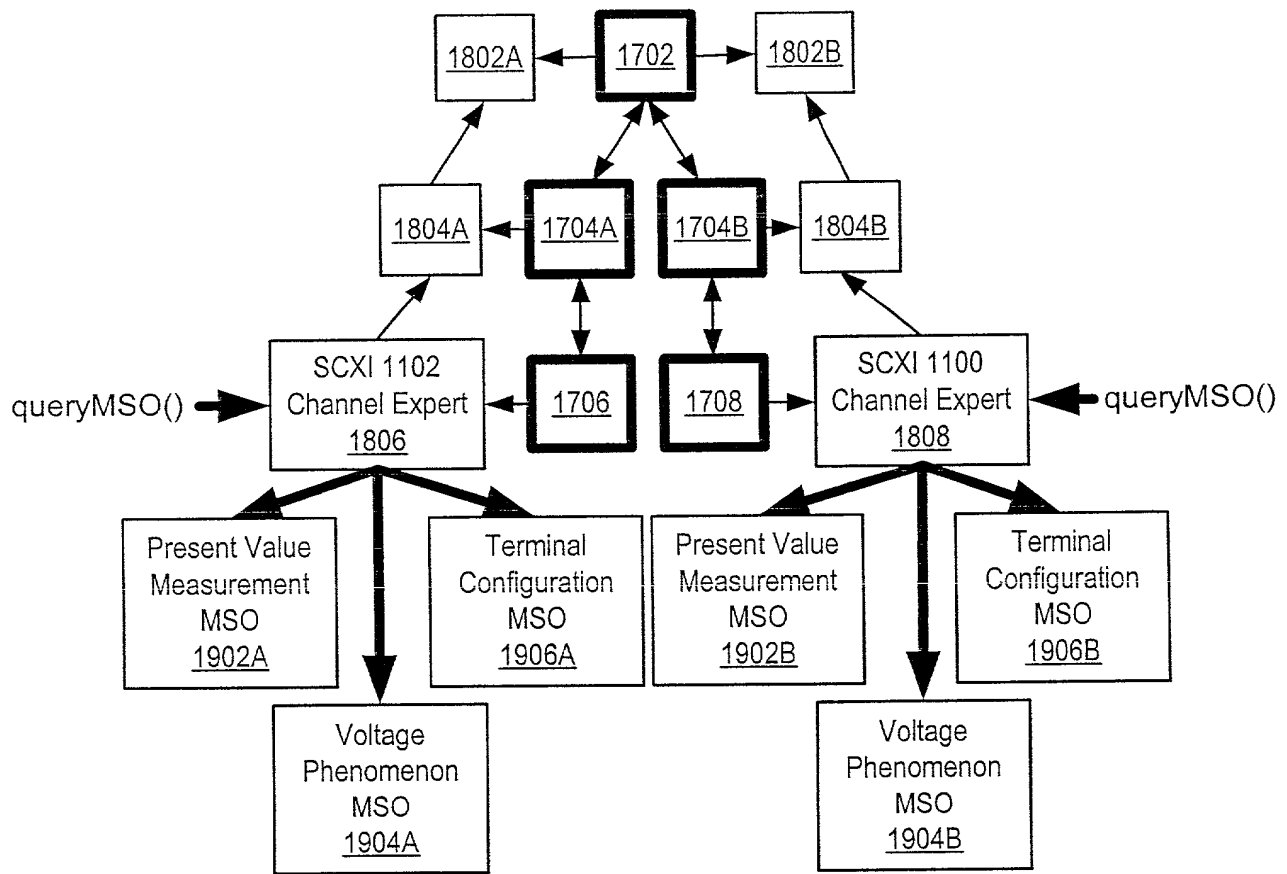


Figure 17





Deserialize Named Channel MSOs

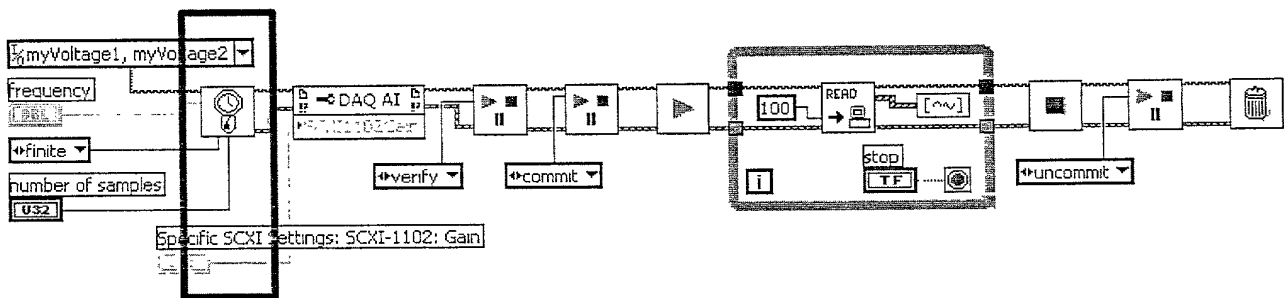
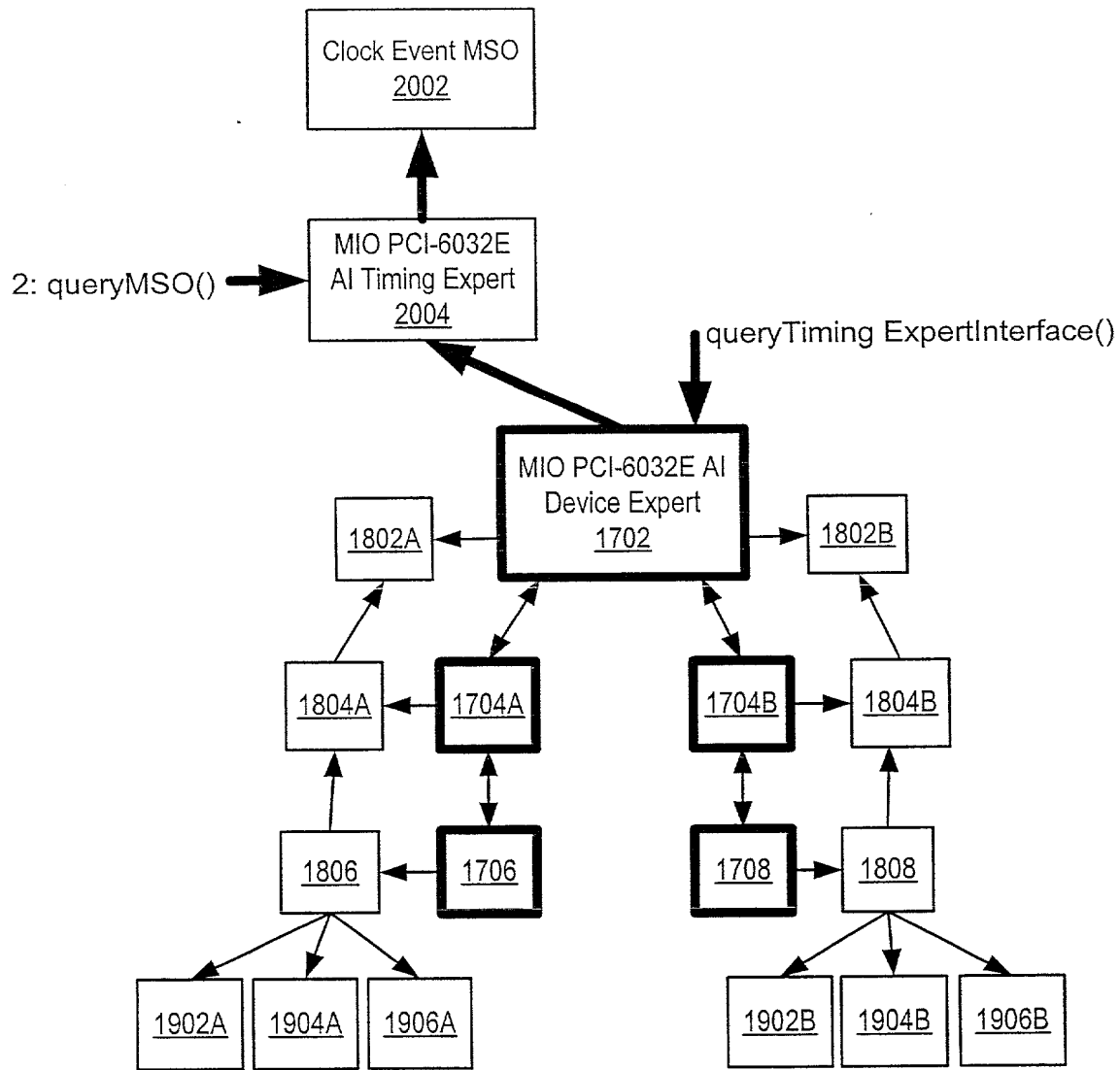


Figure 19



Configure Timing Experts

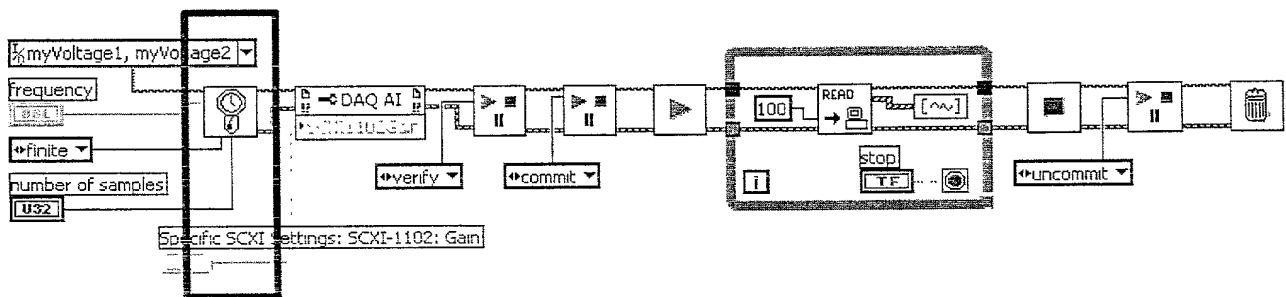
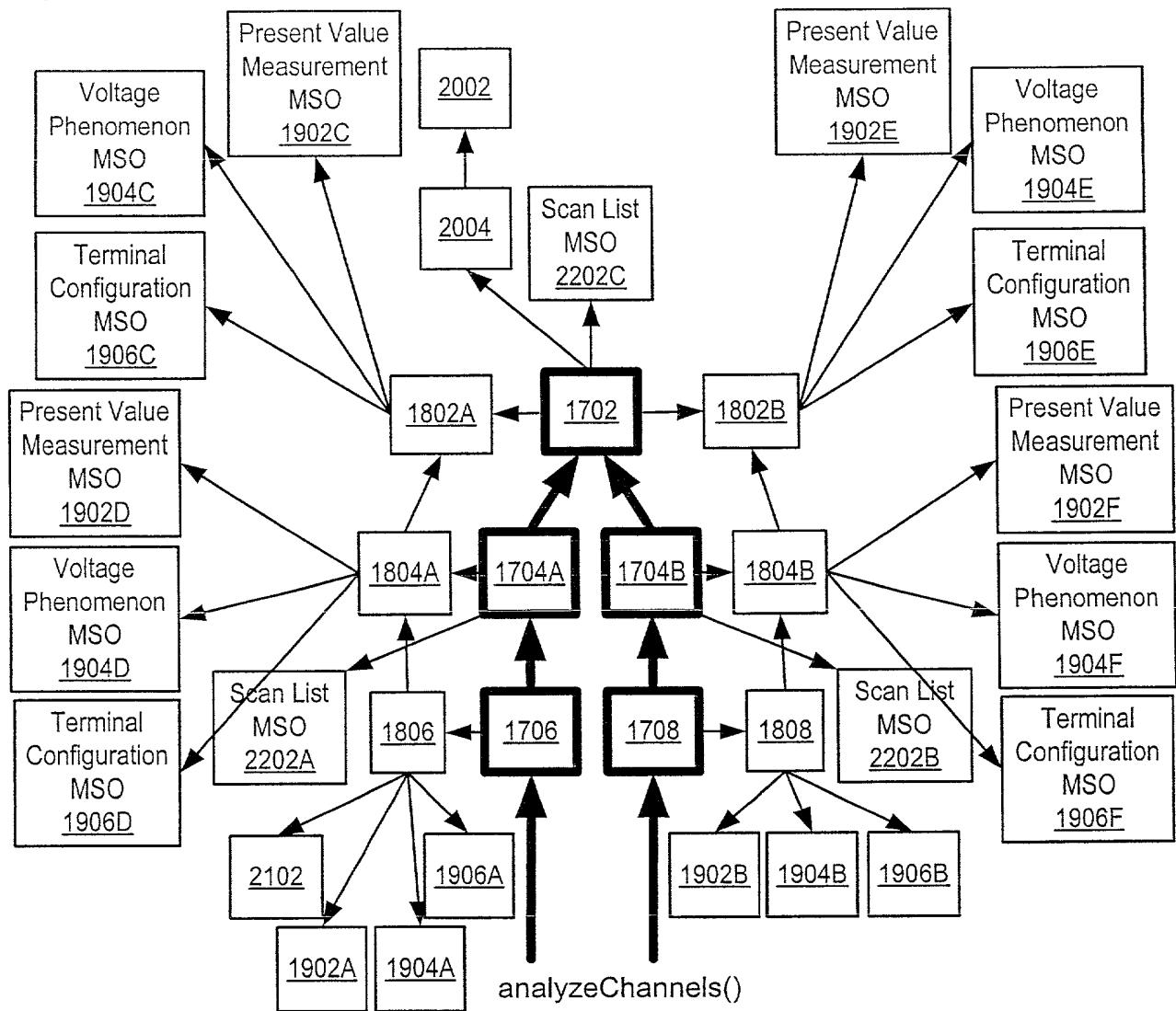


Figure 20





Analyze Channels

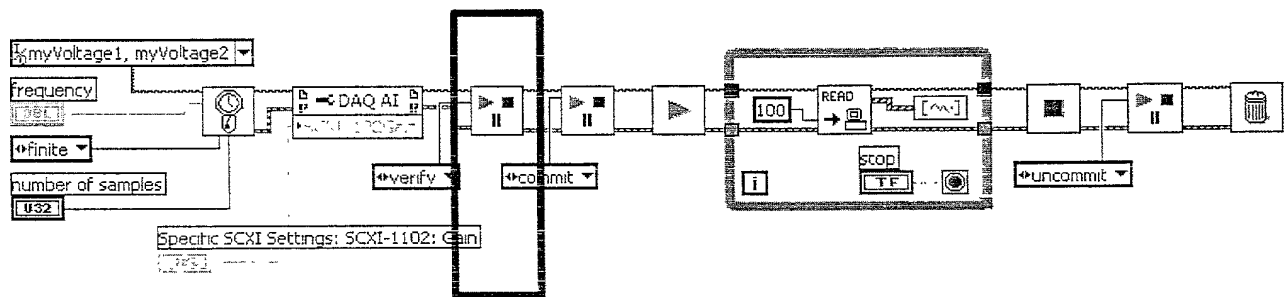
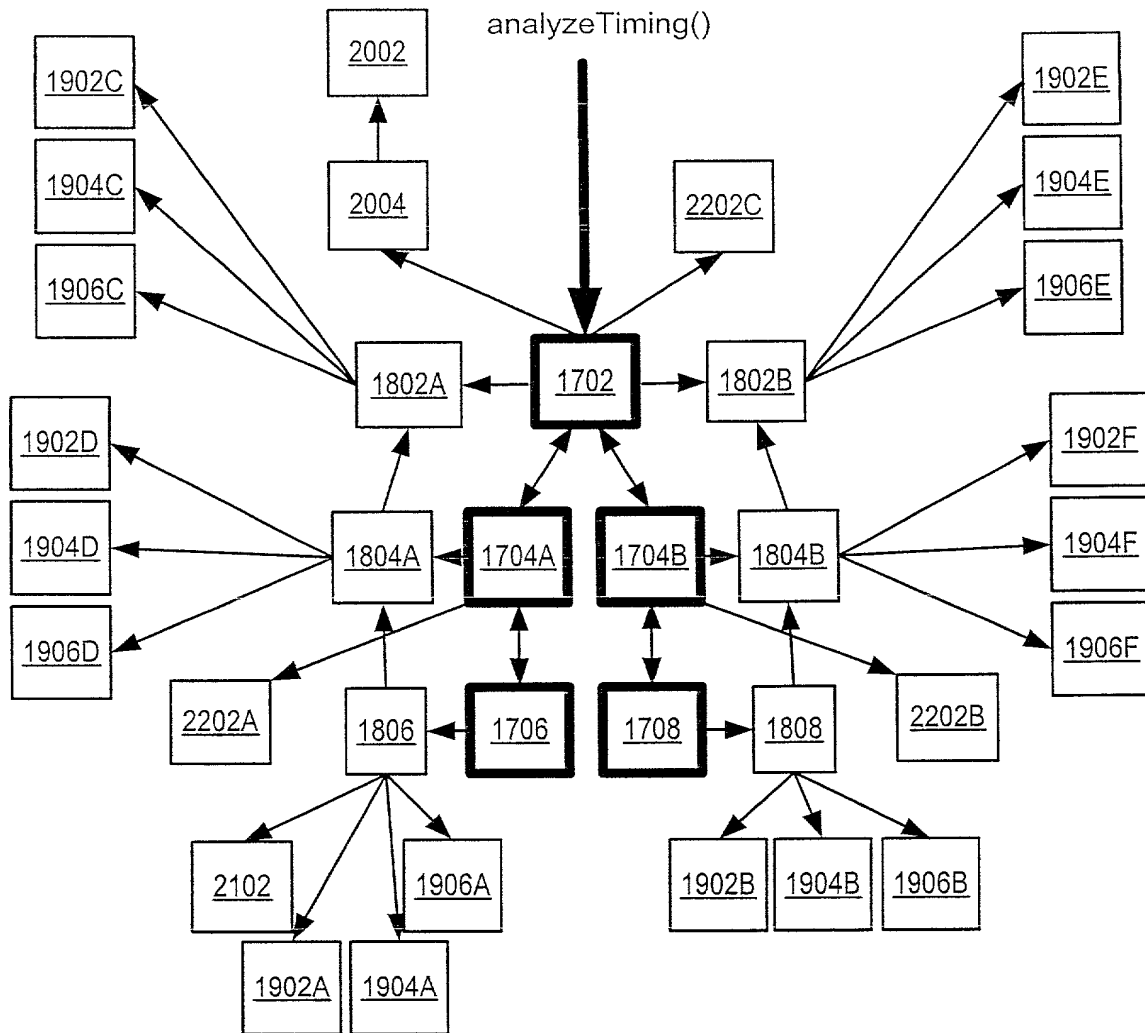


Figure 22



Analyze Timing

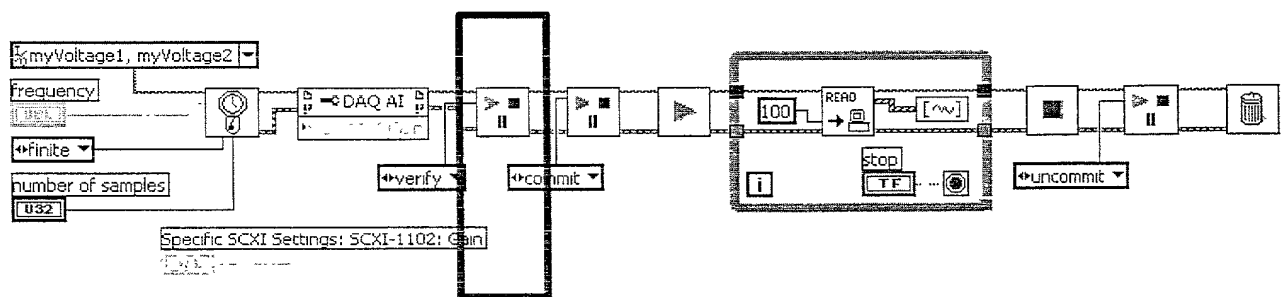
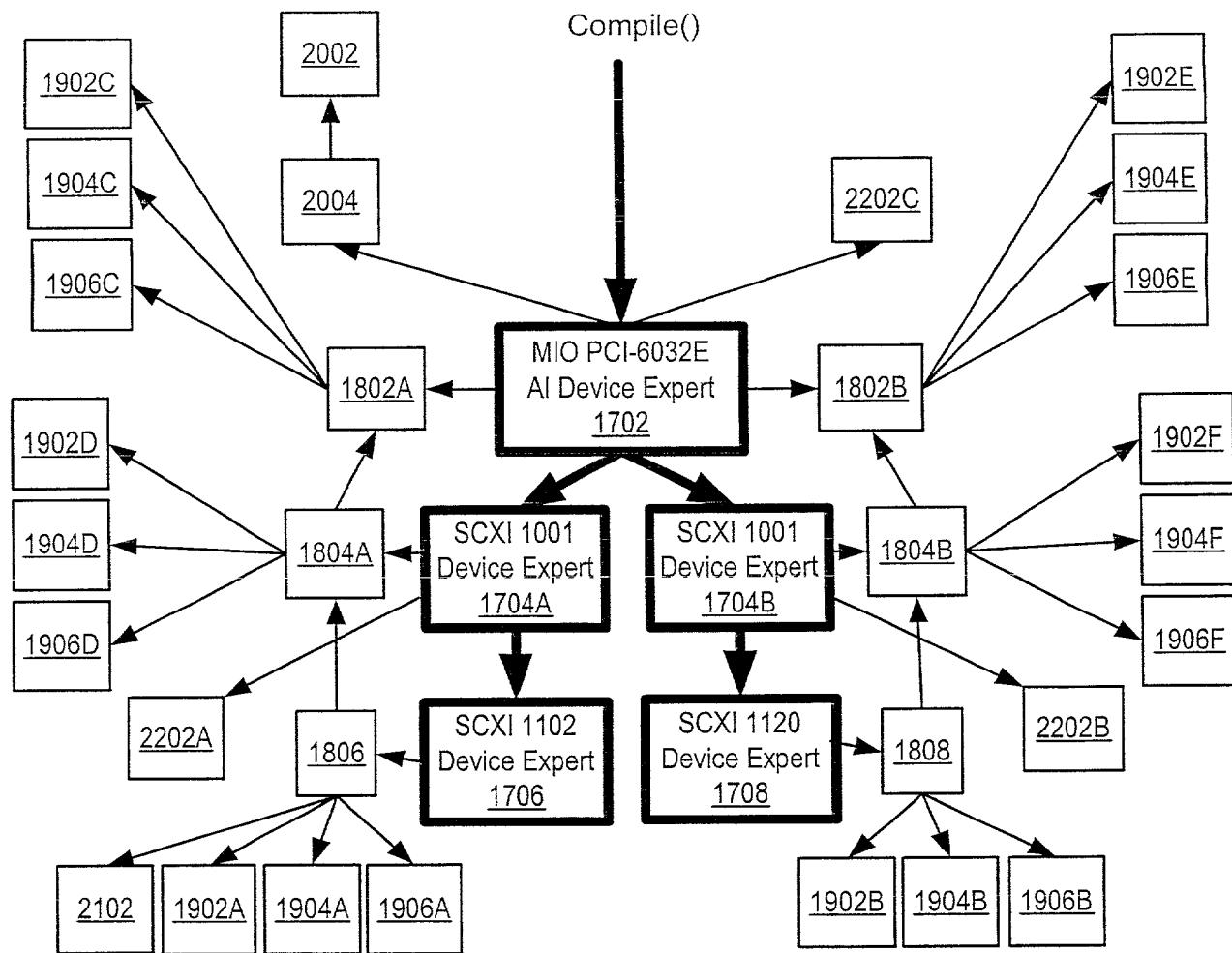


Figure 23





Compile

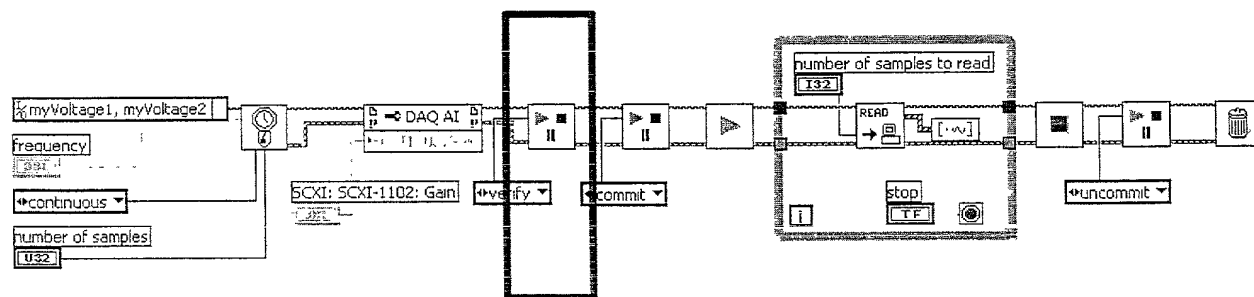
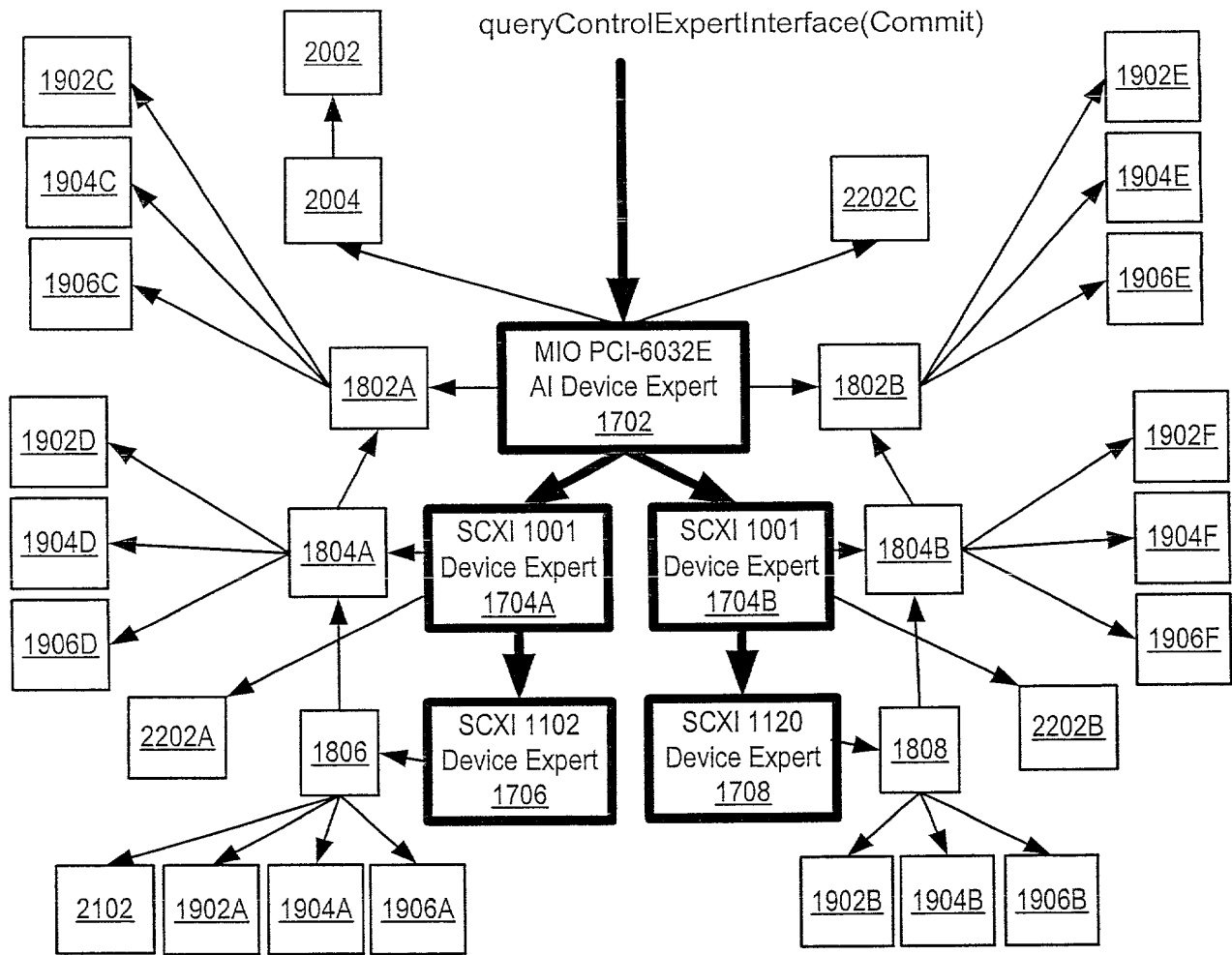


Figure 24A



Commit

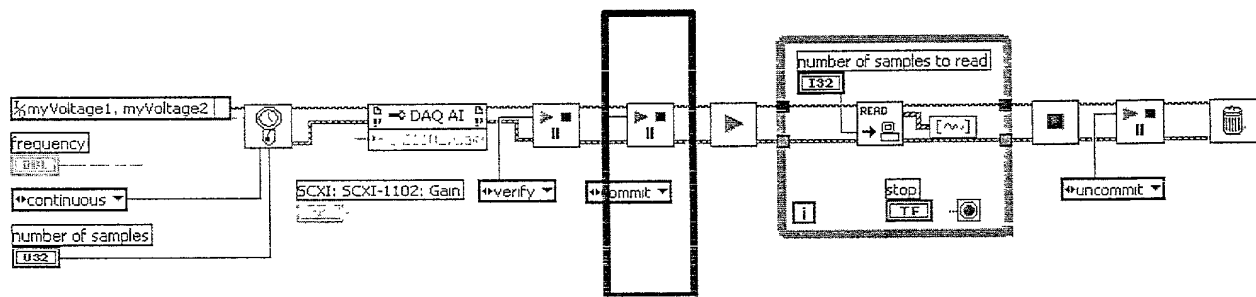
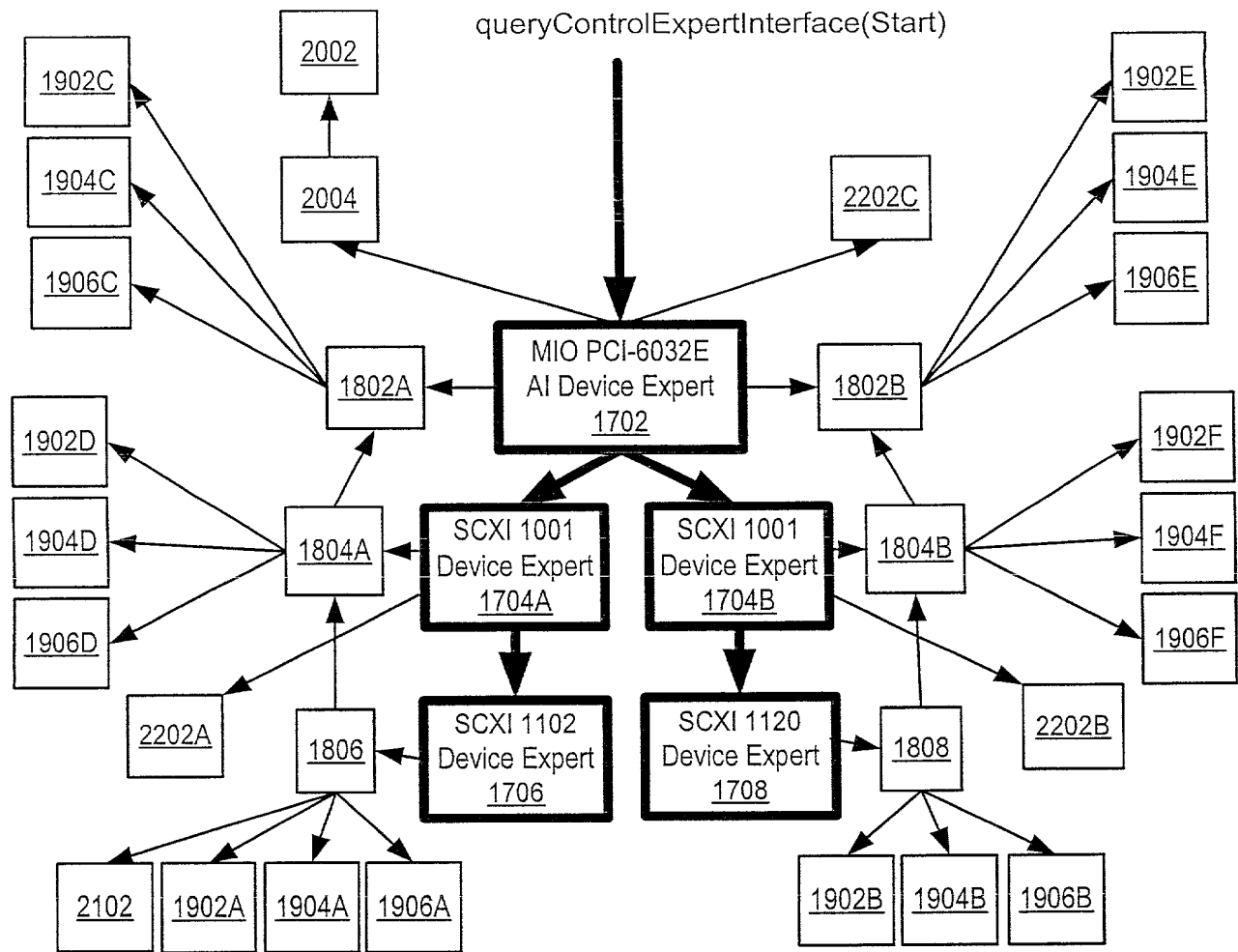


Figure 24B



Start

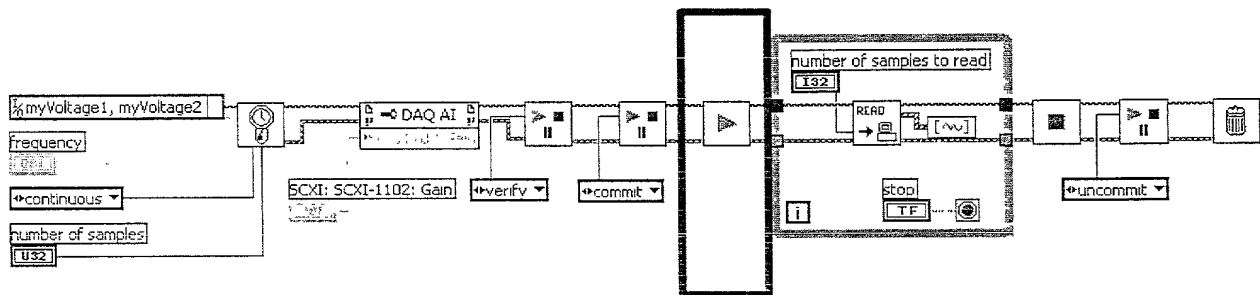


Figure 24C

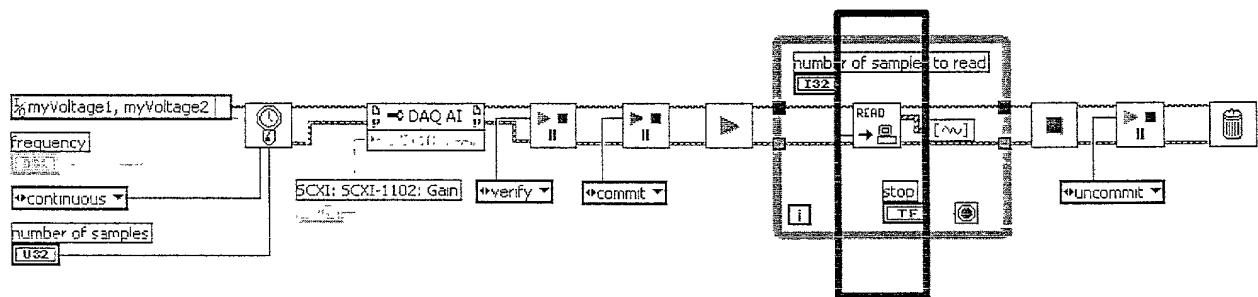
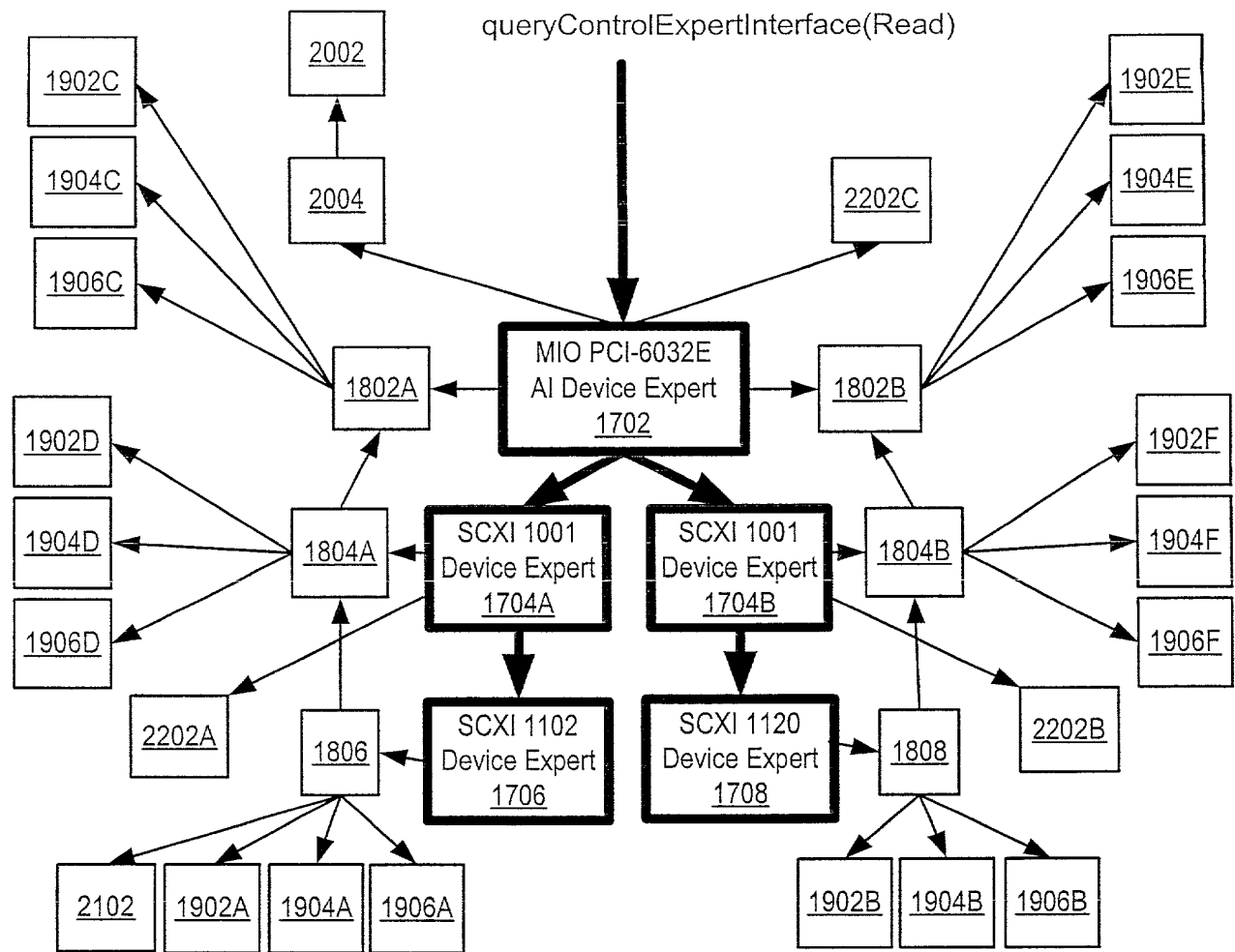
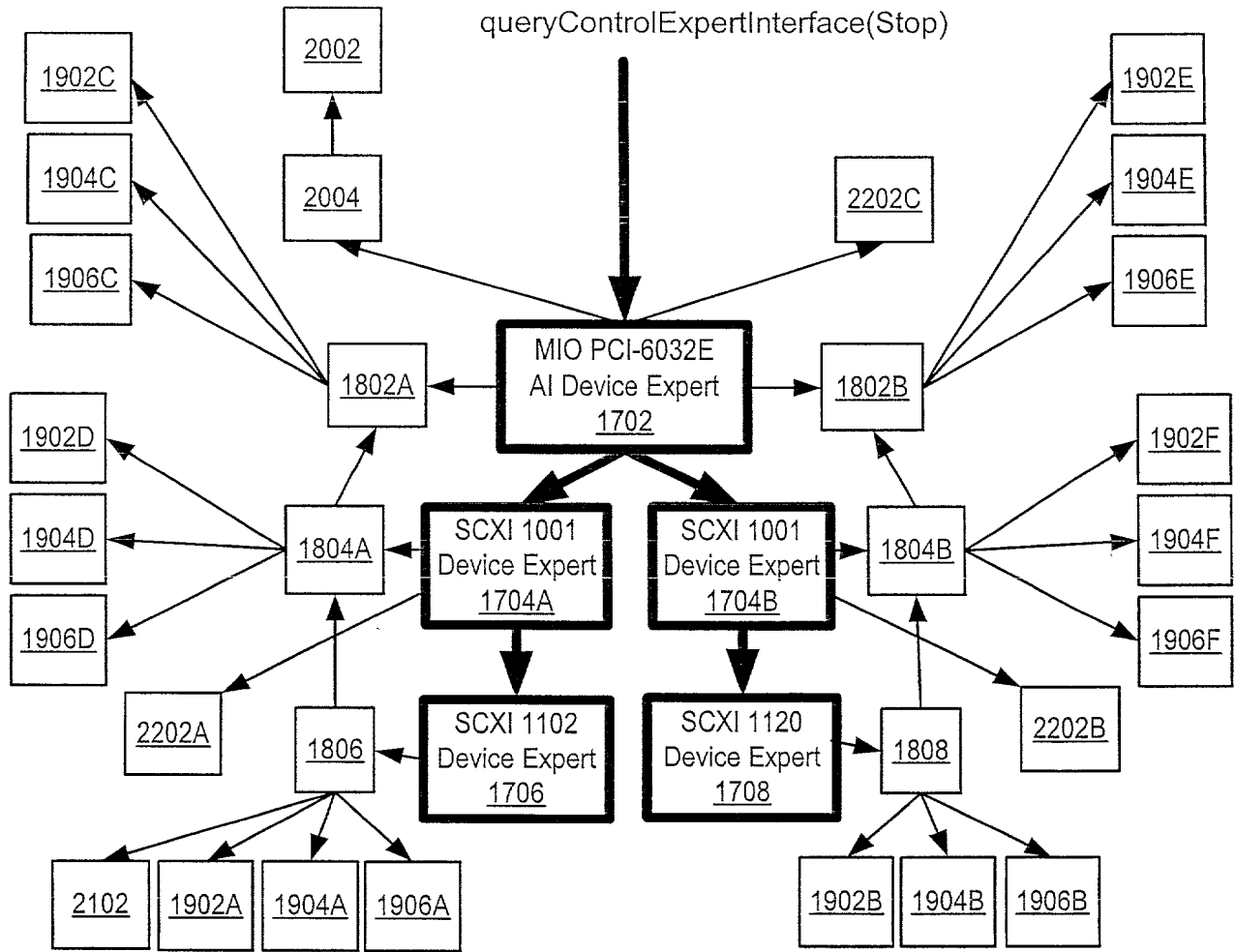


Figure 24D



Stop

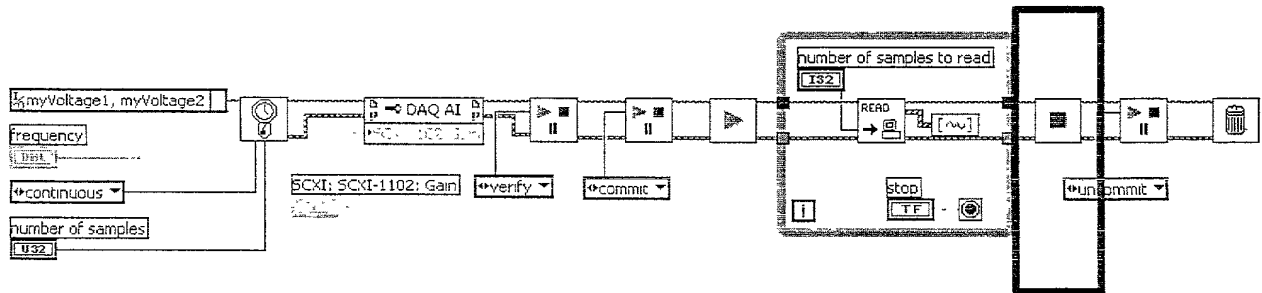
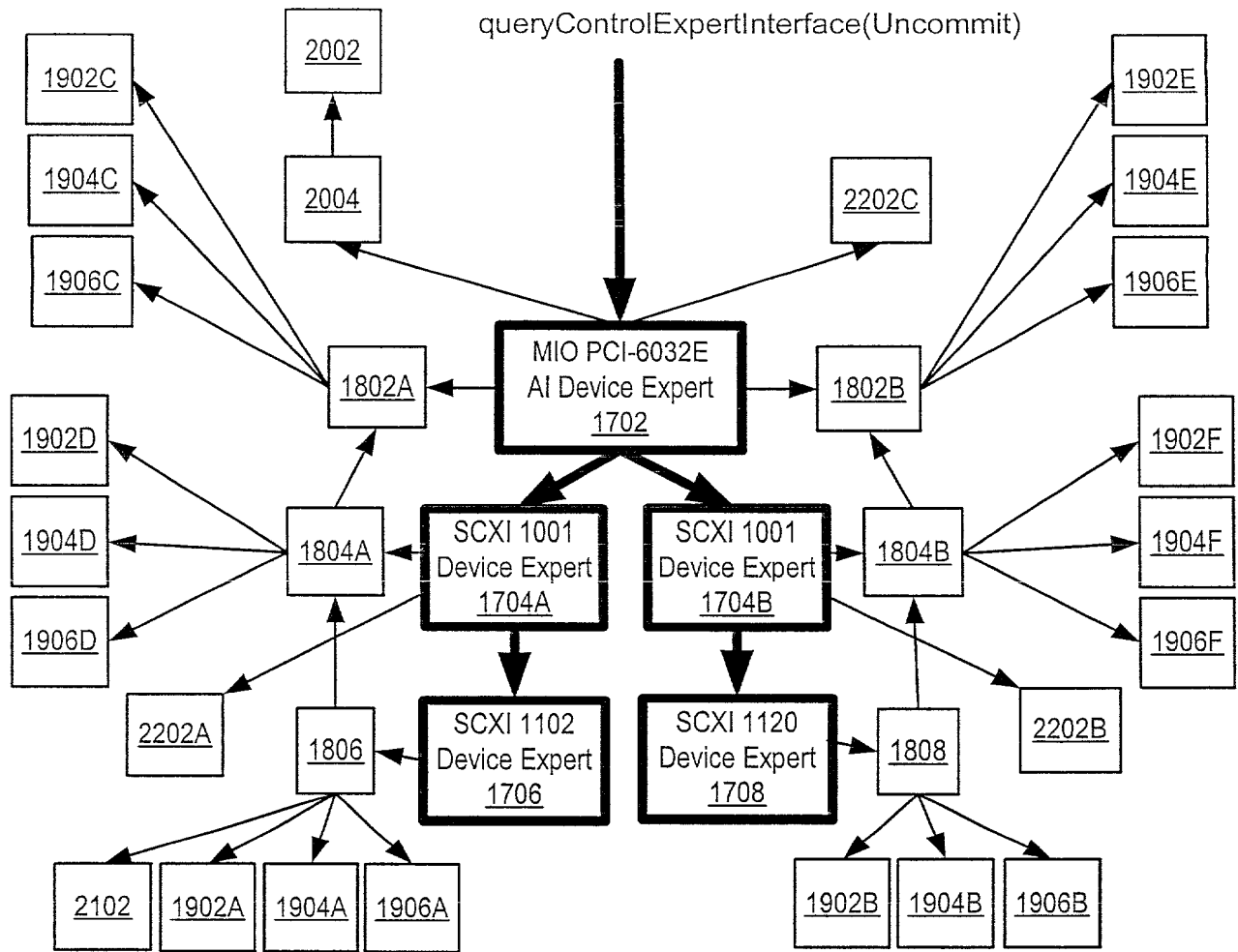


Figure 24E



Uncommit

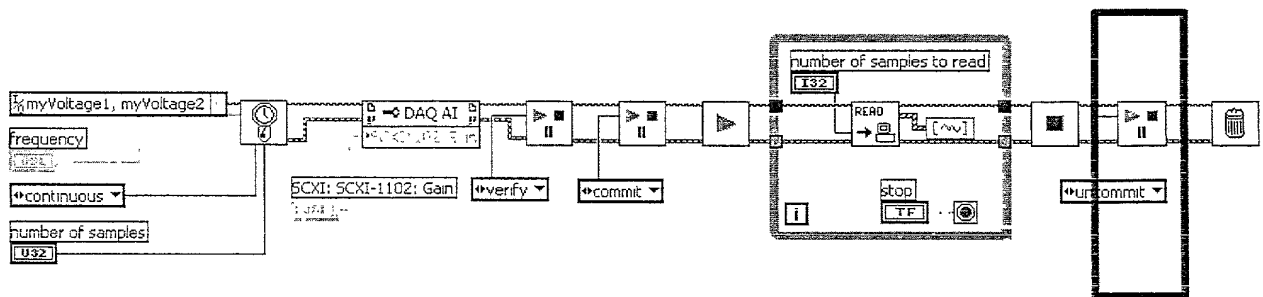


Figure 24F

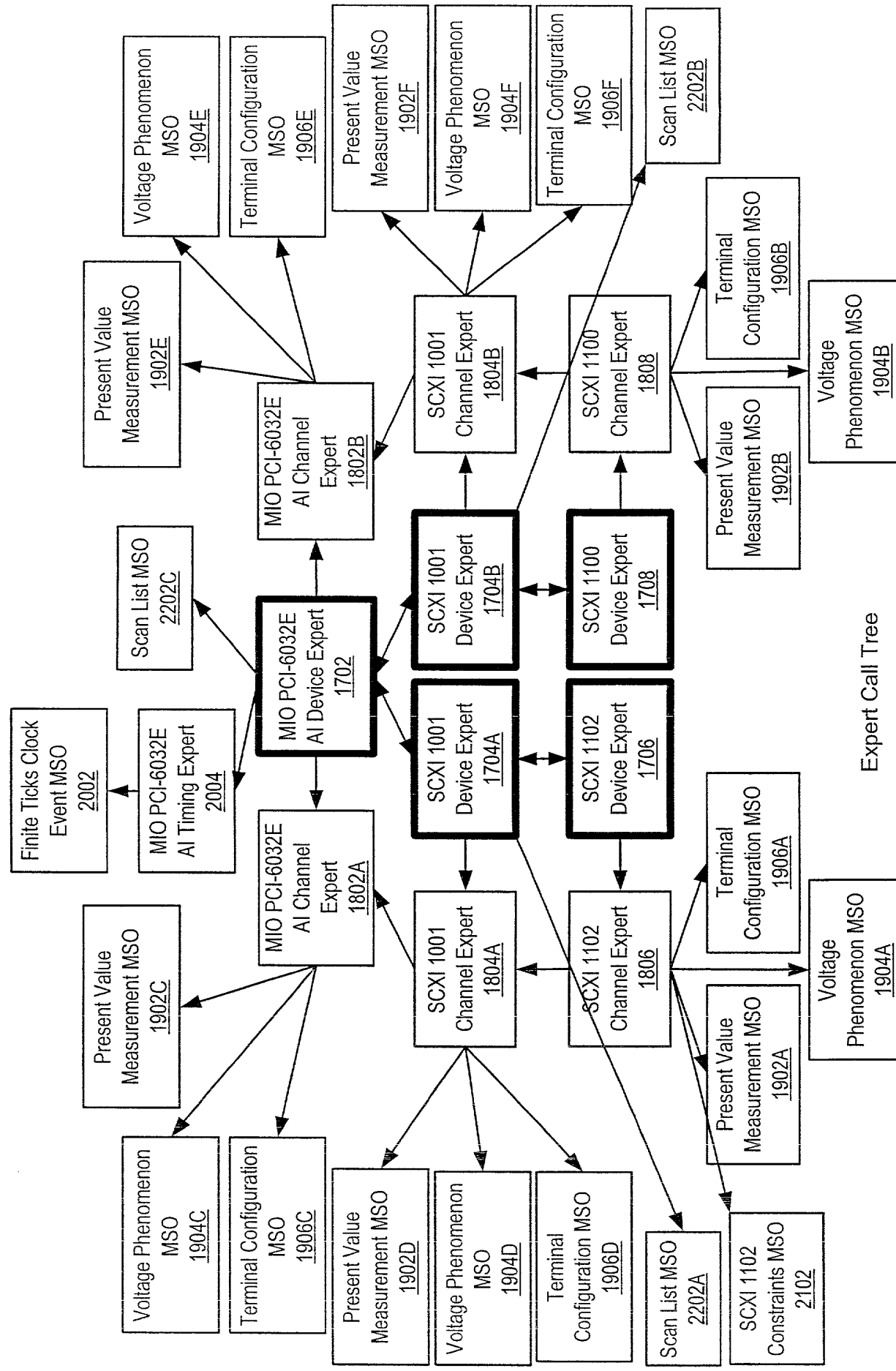


Figure 25

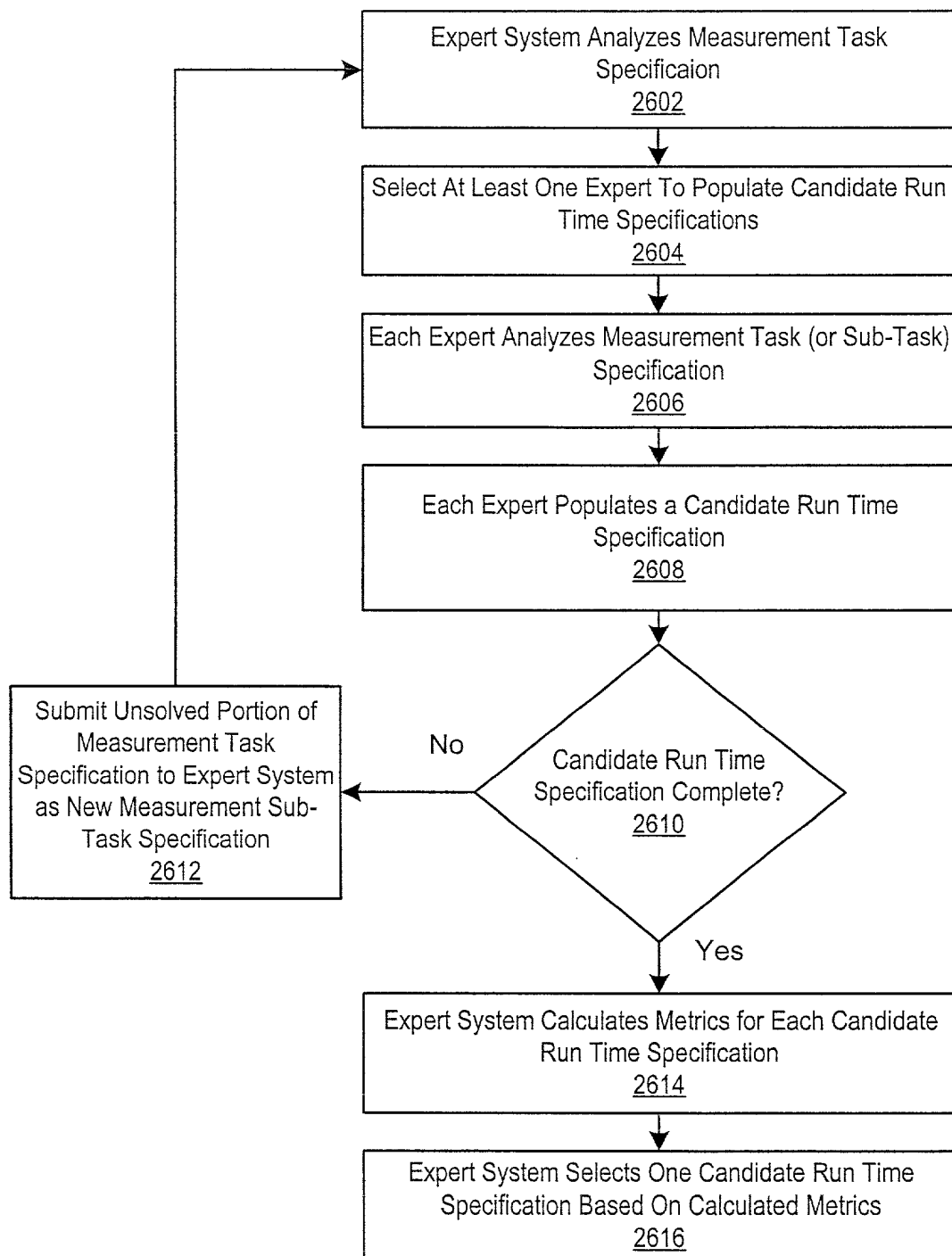


Figure 26



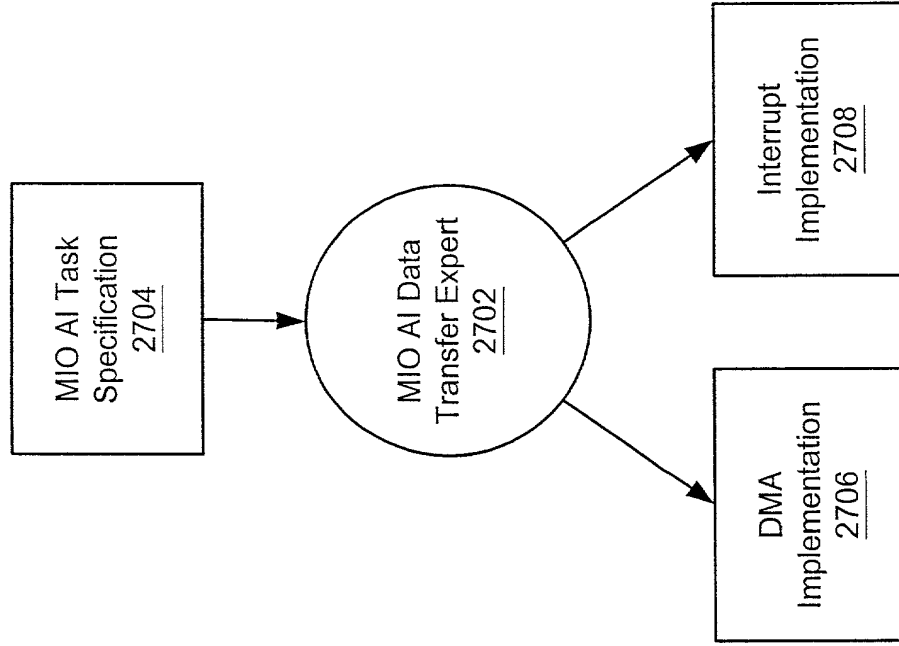


Figure 27

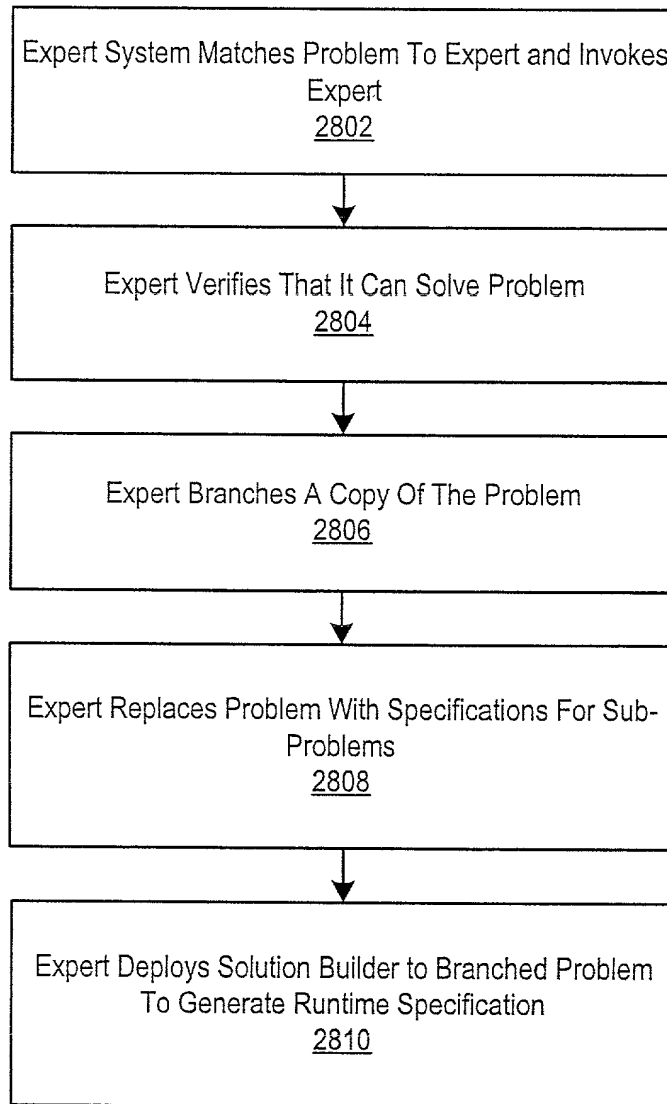


Figure 28

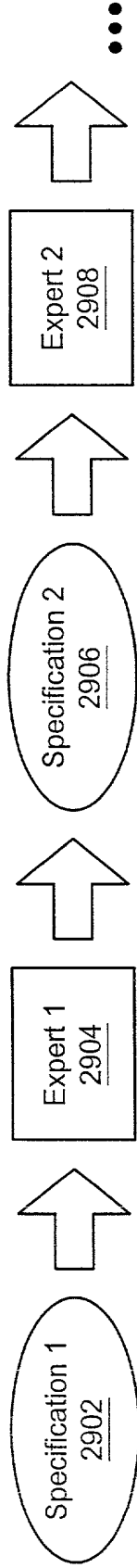


Figure 29

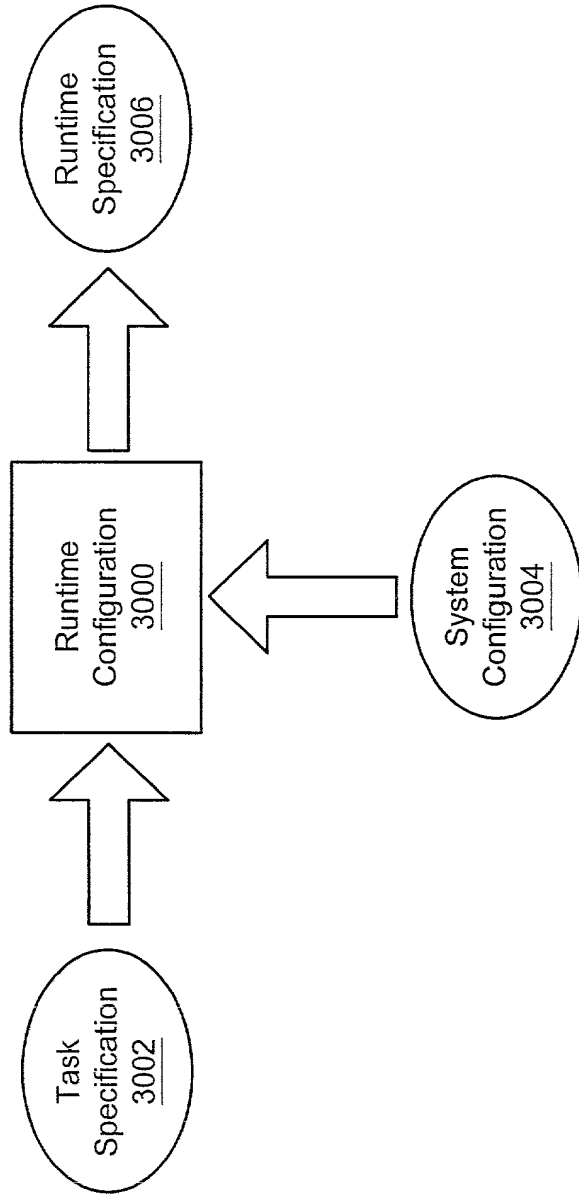


Figure 30

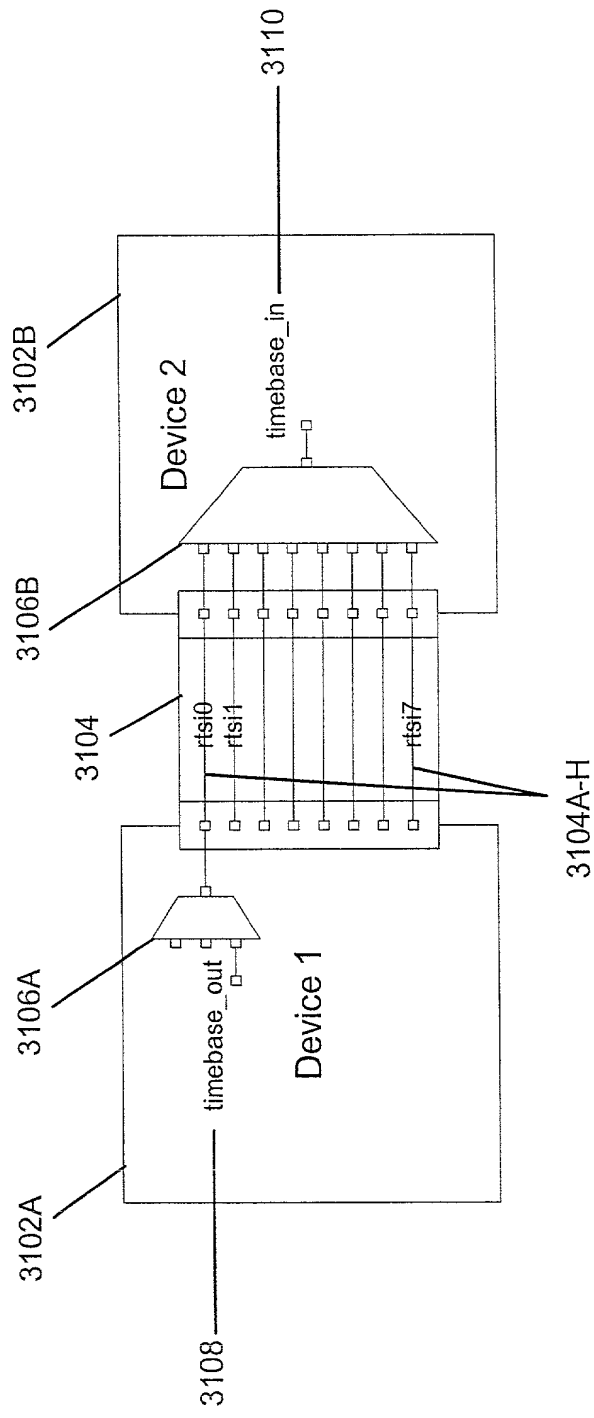


Figure 31

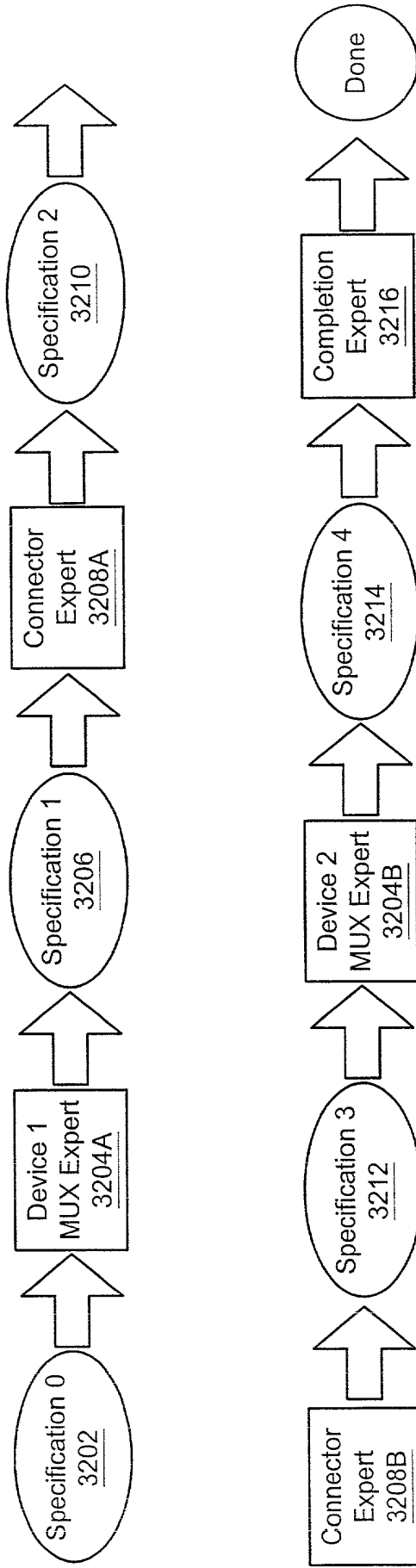


Figure 32

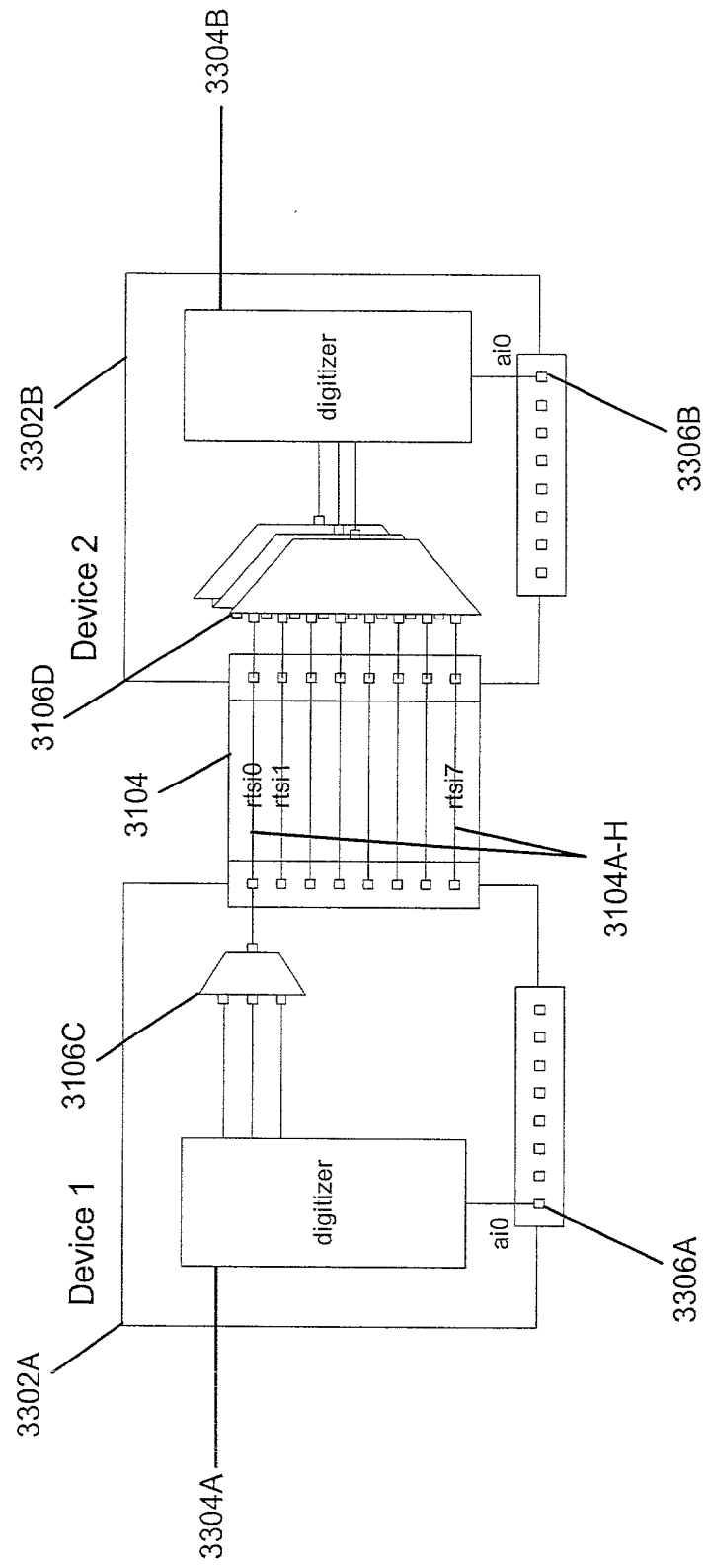


Figure 33





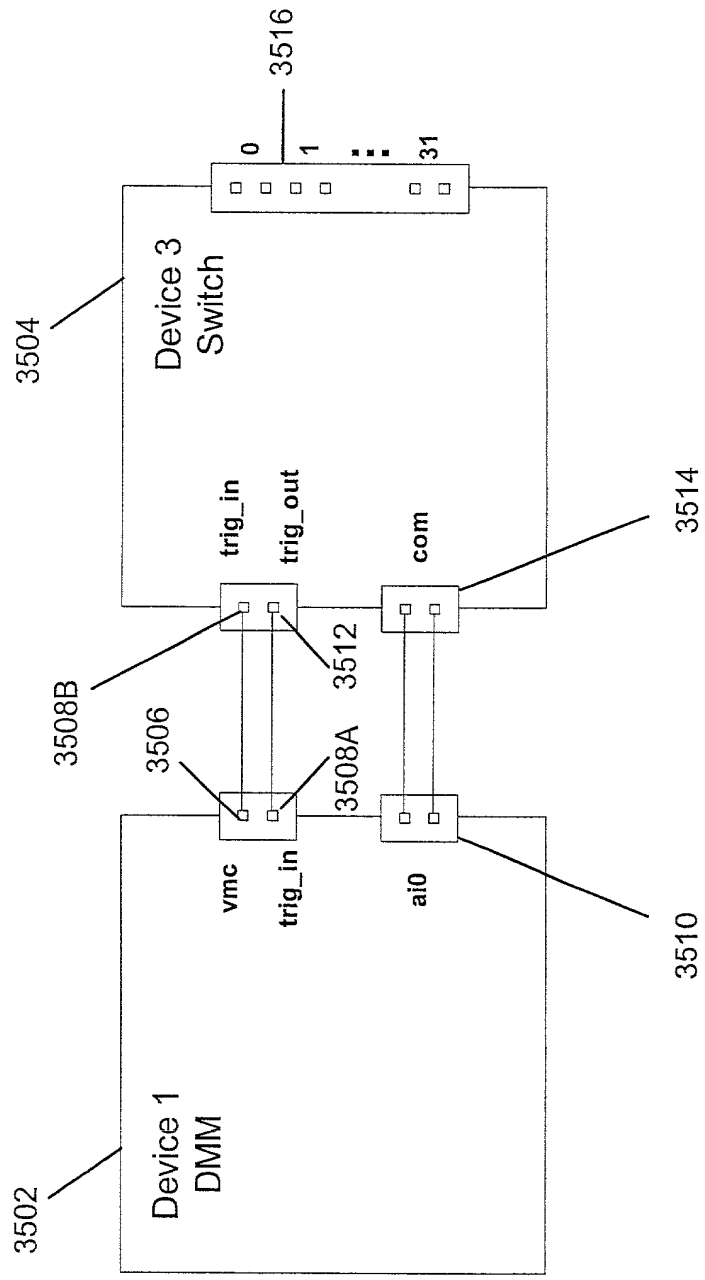


Figure 35

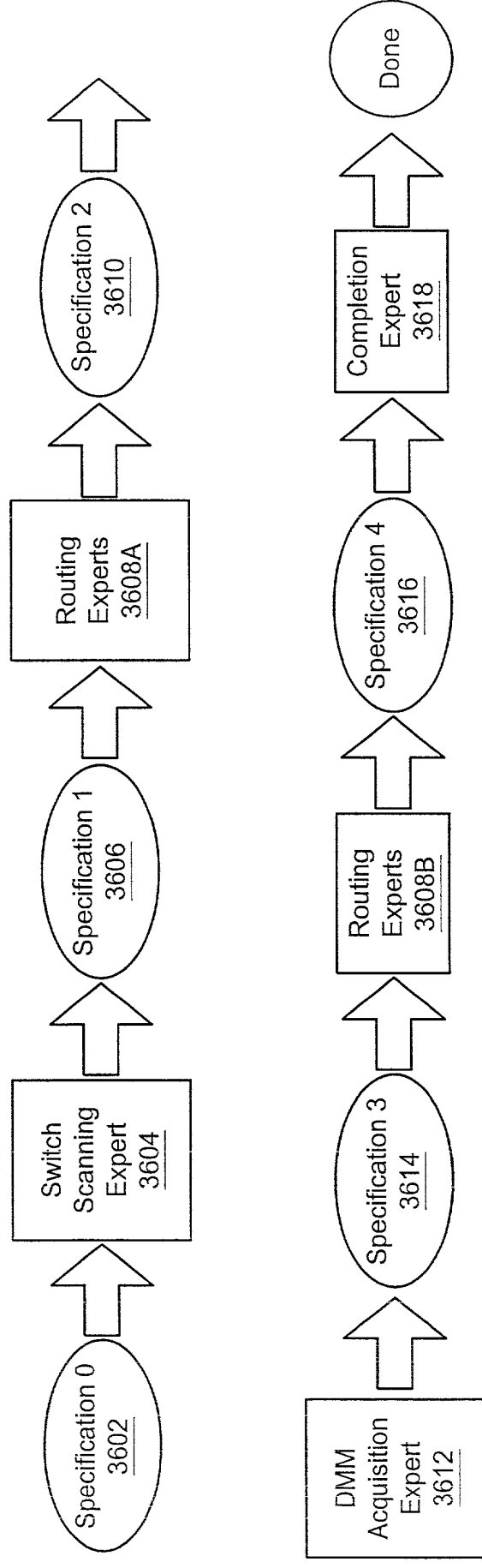
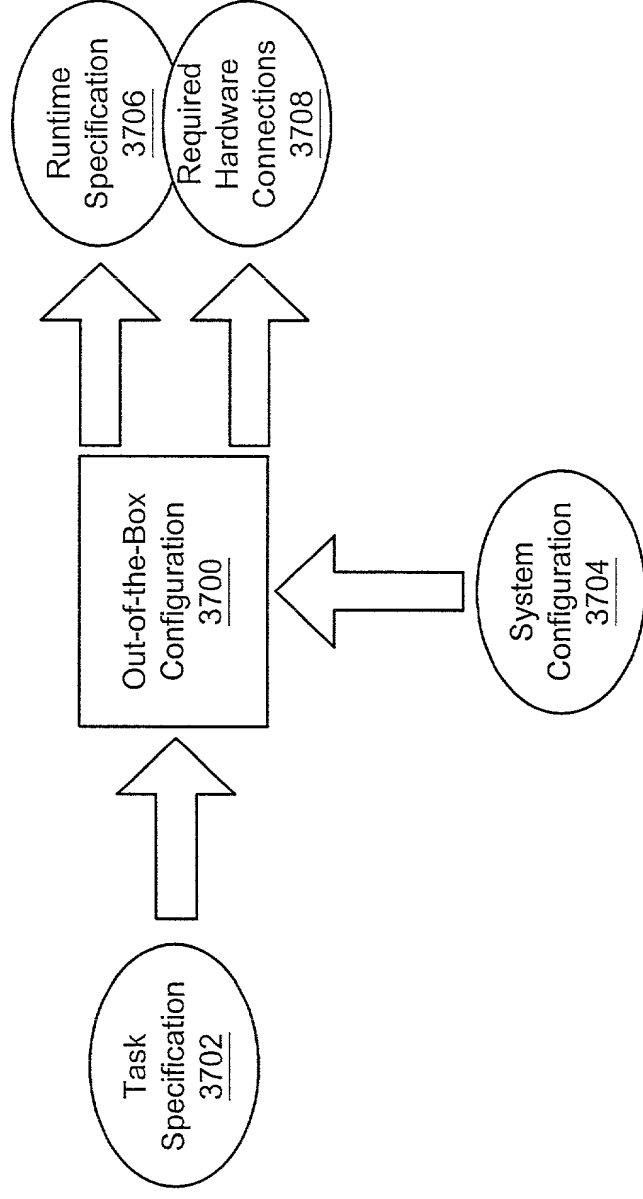


Figure 36



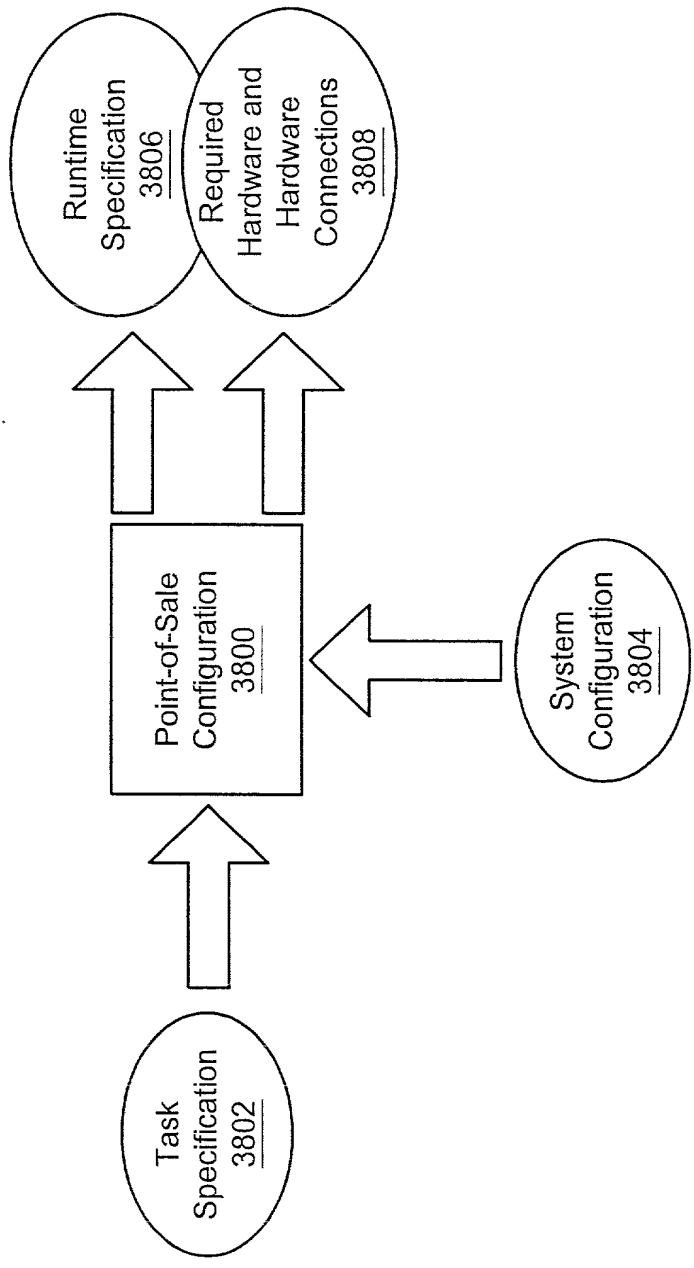
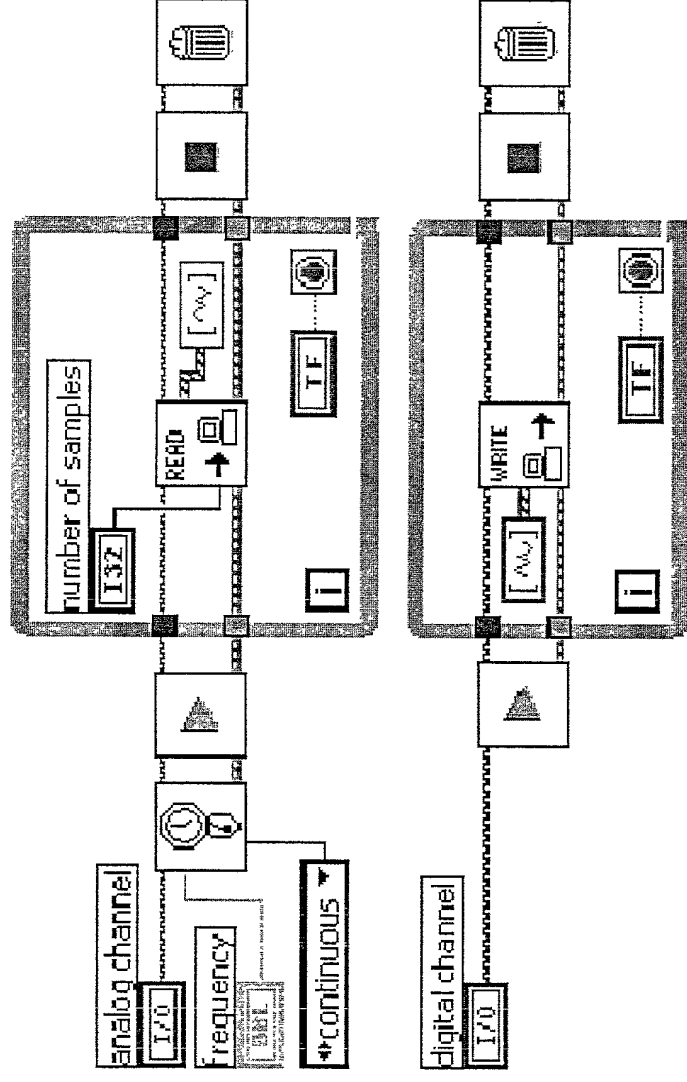


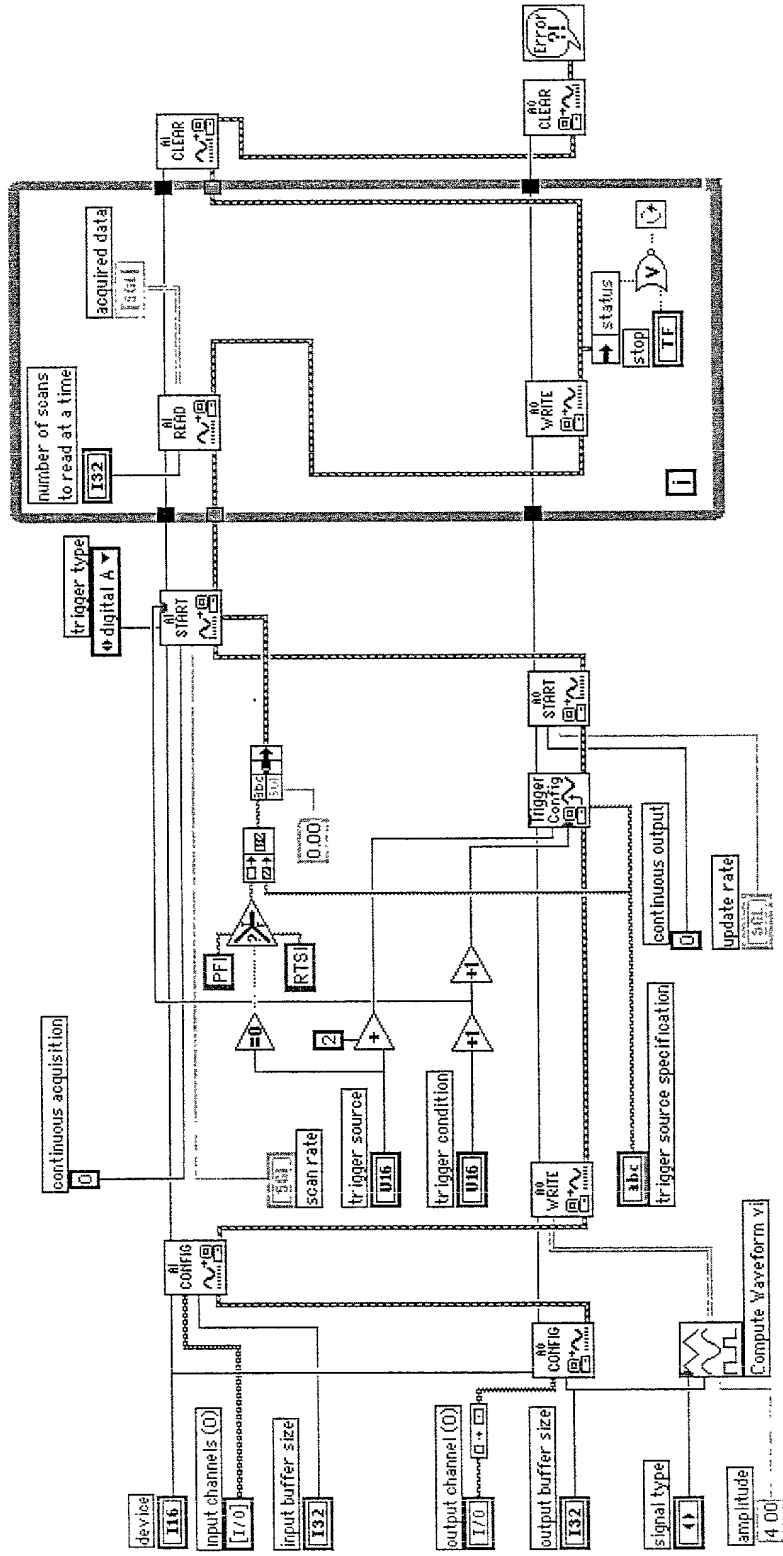
Figure 38





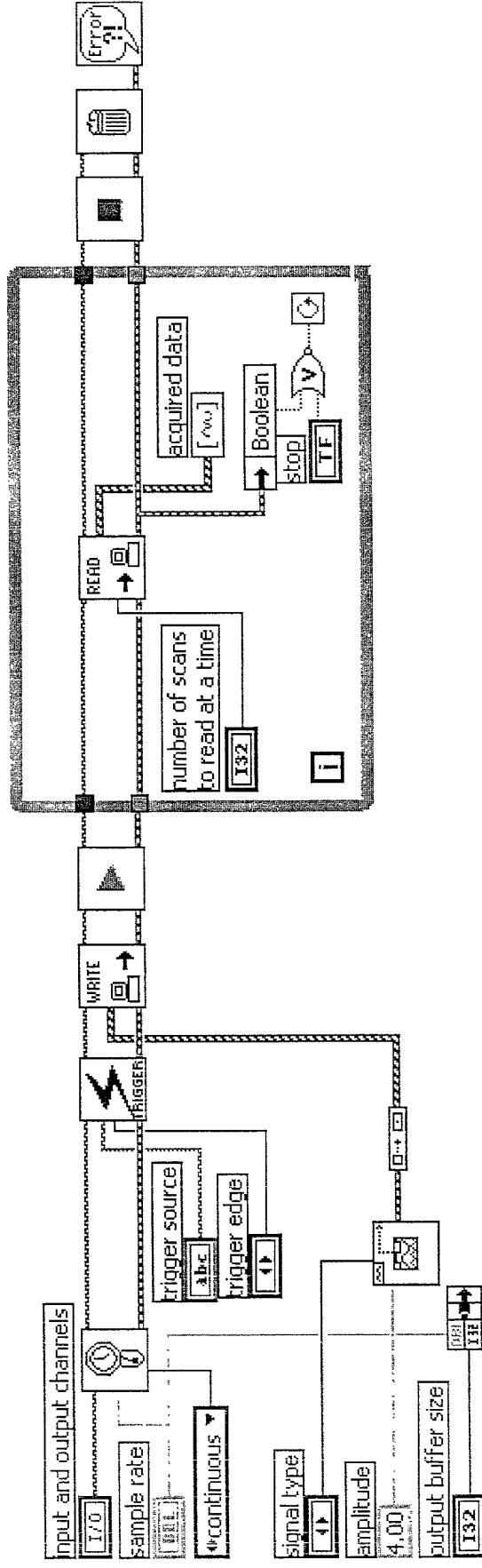
Simultaneous Buffered Analog Input And Single Point Digital Output With Multi-Threaded Driver

Figure 39B



Simultaneous Triggered Buffered A/AO (Prior Art)

Figure 40A

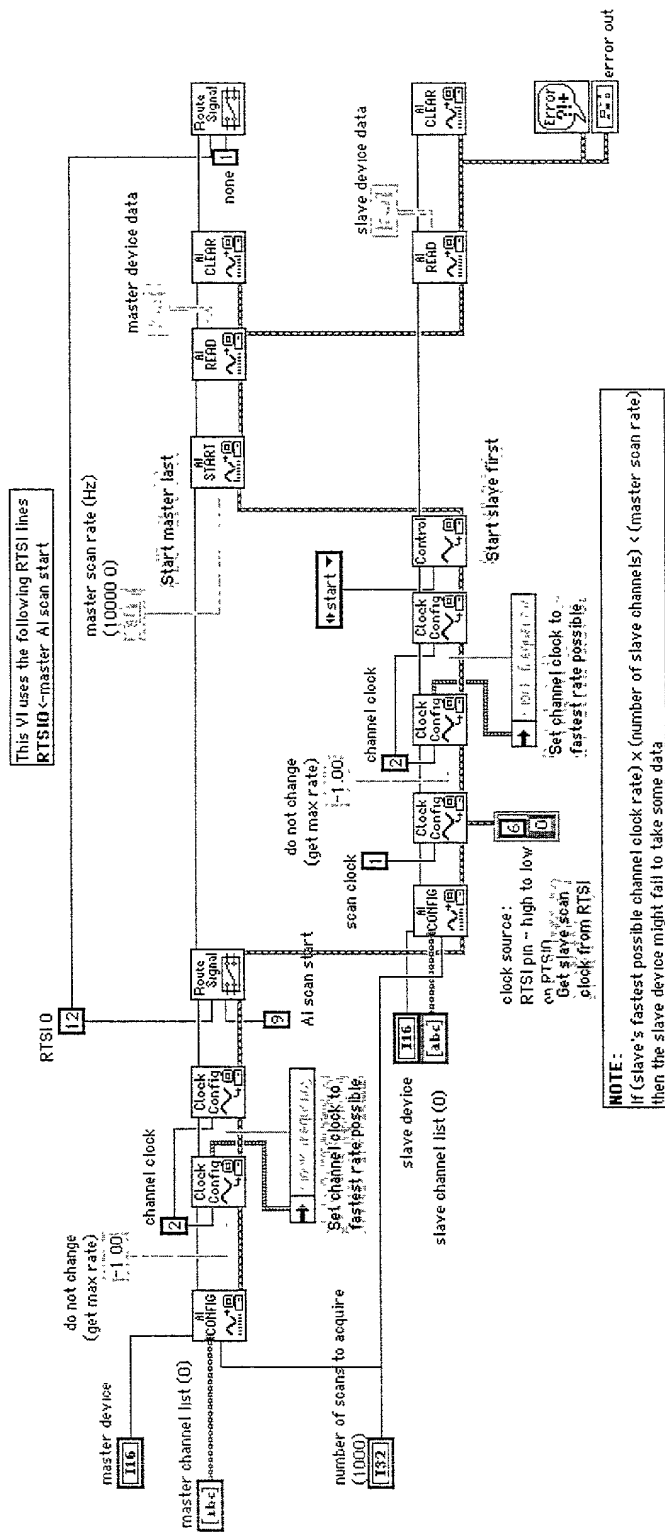


Simultaneous Triggered Buffered A/D Conversion

Figure 40B



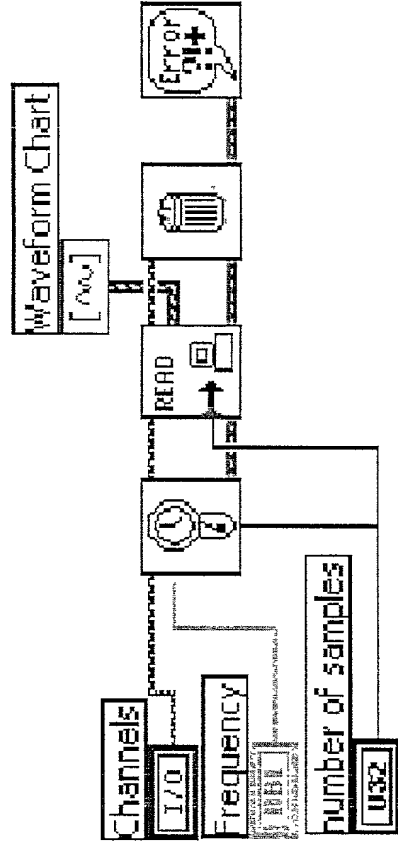
Figure 41A: Sharing Scan Clock Across Two E-Series Devices (Prior Art)



Sharing Scan Clock Across Two E-Series Devices (Prior Art)

Figure 41A

When the device is in the "Error" state, the user can press the "Error" button to view the error message.



Sharing Scan Clock Across Two E-Series Devices

Figure 41B



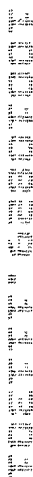


Figure 43A (Prior Art)

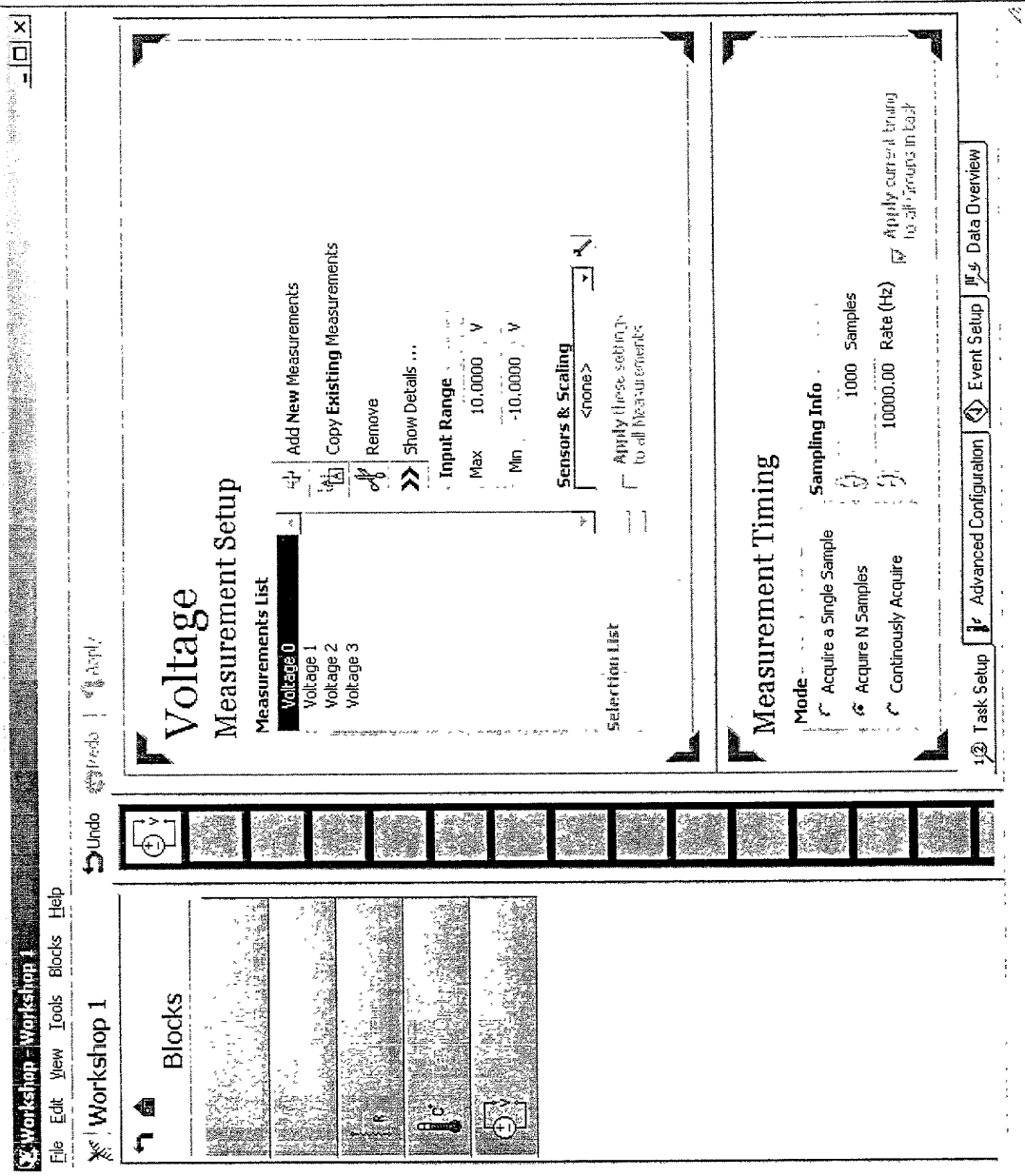
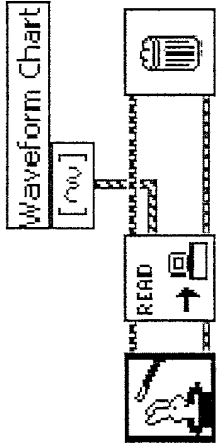


Figure 43B

Figure 43C

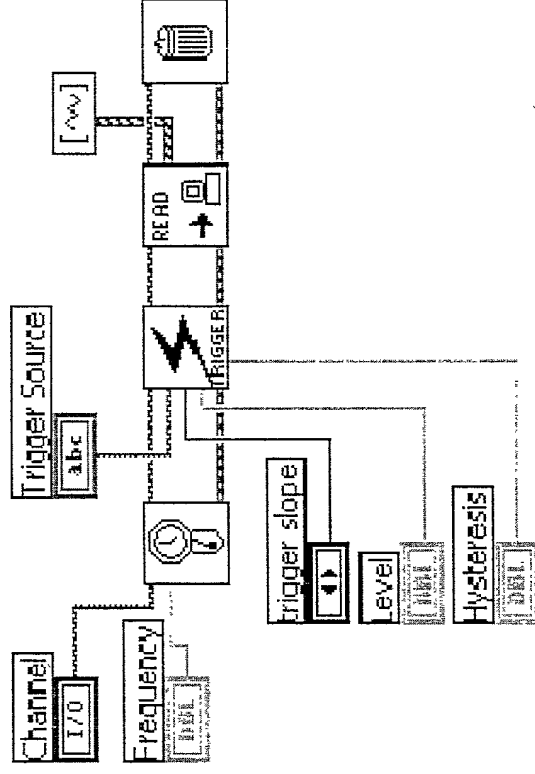


Acquire N Scans External Scan Clock Digital Trigger

Figure 43D



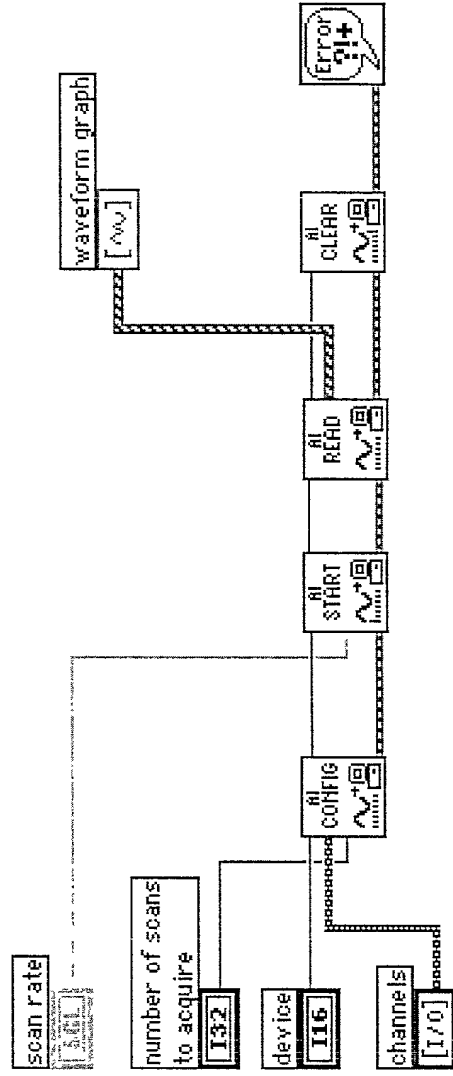




Triggered Acquisition With High Speed Digitizer

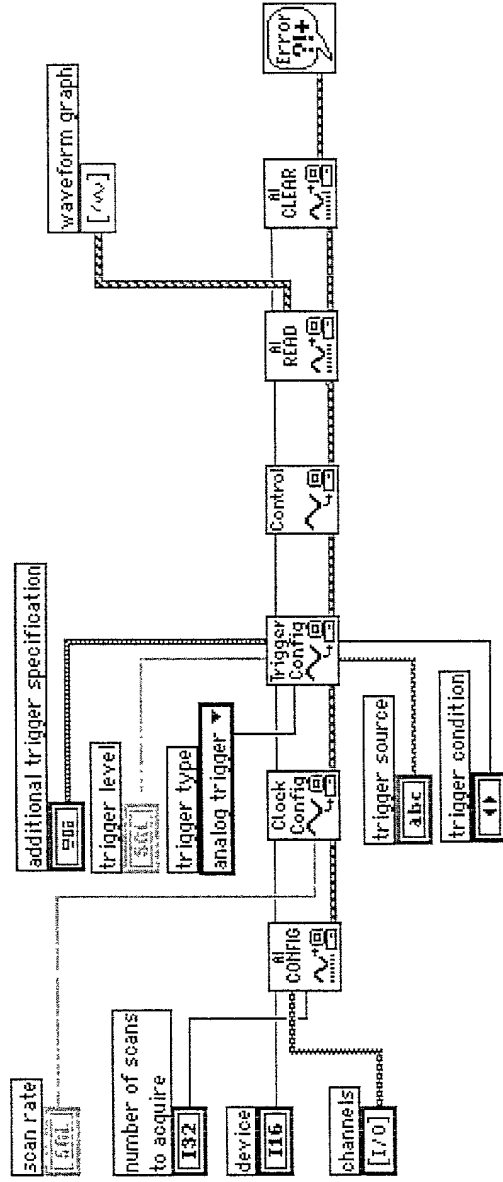
Figure 44B





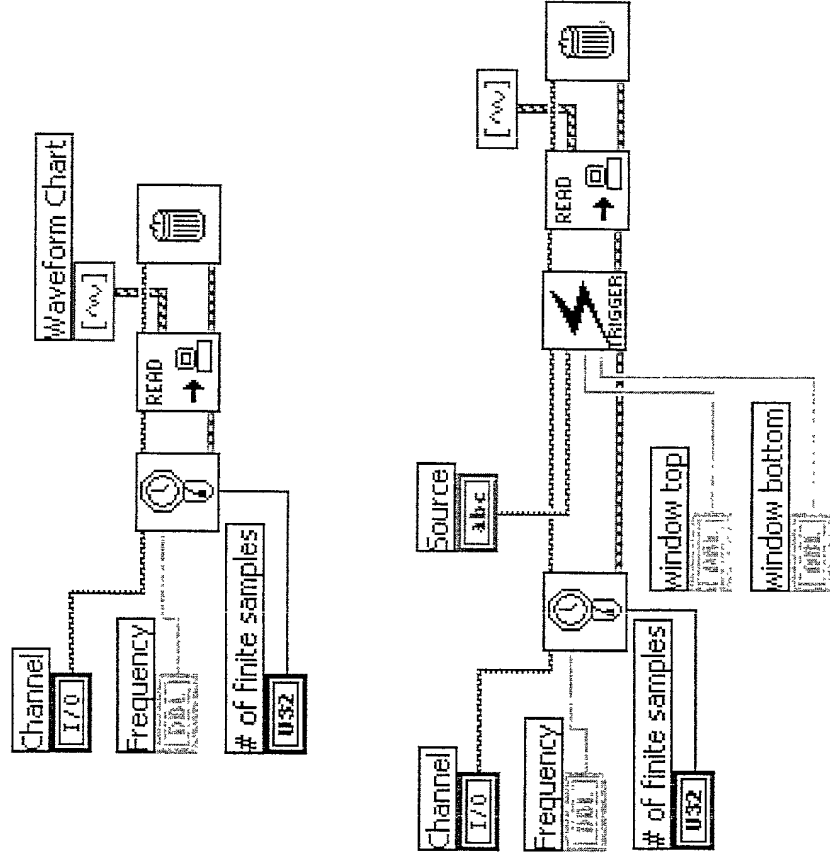
Intermediate Layer (Prior Art)

Figure 45A



Changes For Analog Window Triggering (Prior Art)

Figure 45B



Analog Window Triggering

Figure 45C